PLESSEY
Semiconductors

PRELIMINARY INFORMATION

MV9009 EXP

V21 MODEM TX/RX

The MV9009 is a single chip modulator/demodulator fabricated in silicon gate ISO-CMOS and designed for use in V21 modems. The device can be used alone, or in conjunction with the SL9009 Adaptive Cancellation Filter.

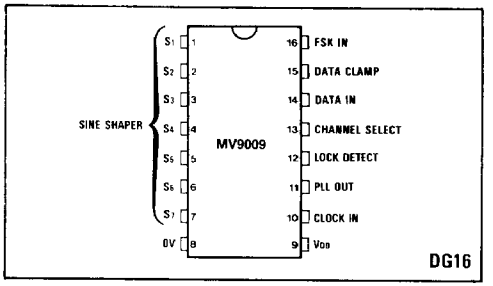


Fig.1 Pin connections - top view

FEATURES

- 300 Baud V21 Operation
- Square or Sinewave Transmit Output Waveforms
- Baseband Shaping to Reduce Out-of-Band Modulation Products
- 2nd Order Digital PLL Receiver
- Lock Detect Output
- Off-Chip Post Detection Filter Enables Optimisation of Received Data Jitter
- Meets R20/SCVF Specification when used with SL9009

ABSOLUTE MAXIMUM RATINGS

Operating temperature	0° C to +70° C
Storage temperature	-65° C to +150° C
Supply voltage range	-0.3V to +7V
Input voltage range	-0.3V to V_{DD} +0.3V
Output voltage range	-0.3V to V_{DD} +0.3V

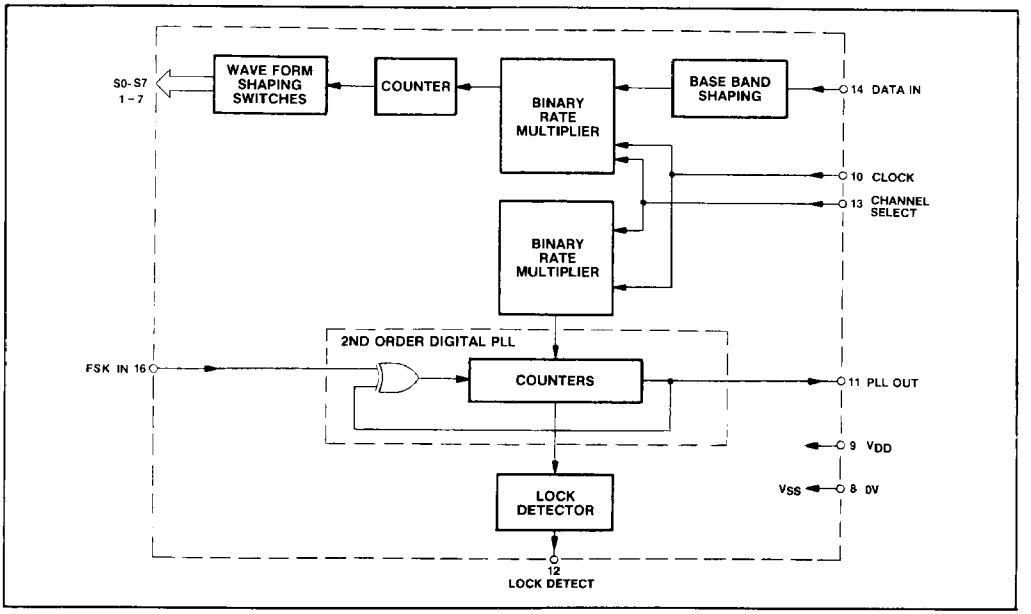


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25° C All potentials referred to pin 8

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply						
Voltage	9	4.5	5	5.5	V	For defined parametrics 0° C to +70° C
Current	9			2	mA	7.5MHz clock V_{DD} = 5.25V
	9			100	μA	Static
Clock input	10					
Input voltage high		3.3			V	V_{DD} = 4.75V
Input voltage low				1.58	V	V_{DD} = 5.25V
Input current				20	μA	V_{DD} = 5.25, V_{IN} = 5.5V
Other inputs	13,14,15,16					
Input voltage high		1.8			V	V_{DD} = 4.75V
Input voltage low				0.9	V	V_{DD} = 5.25V
Input current				20	μA	V_{DD} = 5.25V, V_{IN} = 5.5V
Hysteresis		30			mV	
Sine outputs (open drain)	1,2,3,4,5,6,7					
$R_{DS\ (ON)}$		20	32	47	Ω	V_{DD} = 4.75V
$\Delta R_{DS\ (ON)}$				10	Ω	I_{OL} = 5mA, V_{OL} = 0.5V
Lock detect	12					
Output voltage high		4.27			V	V_{DD} = 4.75, I_O = 4.75mA
Output voltage low				0.525	V	V_{DD} = 5.25V, I_O = 5.25mA
PLL out	11					
Output voltage high		4.995			V	I_O = 25μA, V_{DD} = 5V
Output voltage low				0.005	V	
Output s/c current				50	mA	V_{DD} = 5.25V

OPERATING NOTES

If it is desired to simplify the transmit filtering, the on-chip sine shaping circuit can be used. If this is not needed (for example when using the Reticon R5631 modem filter) then the square wave from pin 4 is used with a pull-up resistor.

The chip produces a sinewave output by scanning an array of 7 resistors as shown in Fig.3. The smallest resistor value should be chosen to be of the order Ron x 1000 ≃ 50kΩ.

Each resistor is successively connected to ground by N-channel MOS transistors within the chip then successively disconnected, as shown by Fig.4. Correct weighting of the resistors should give a sinewave output. If 1% matching of resistors is attained, the worst case distortion will be 2nd harmonic 47dB down on the fundamental. In Fig.4 a '0' indicates a closed switch, a '1' an open switch.

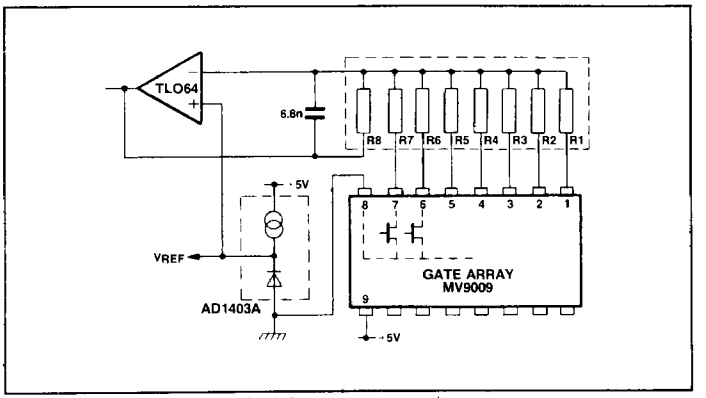
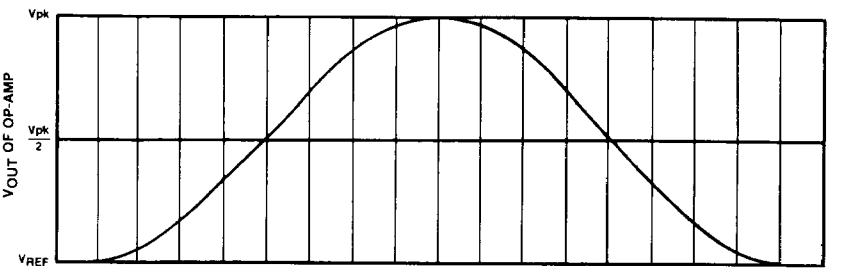


Fig.3 Output array scanning



$V_{ref} - V_{pk} = V_{ref} . R8/(R1 + R2 + R3 + R4 + R5 + R6 + R7)$

	PIN																	
LOB	7	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1
	6	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1
	5	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	4	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
	3	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	2	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
MOB	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Phase	-90°								90°									270°	

Fig.4 16 step sinewave produced by scanning 7 resistors

OPERATING FREQUENCIES

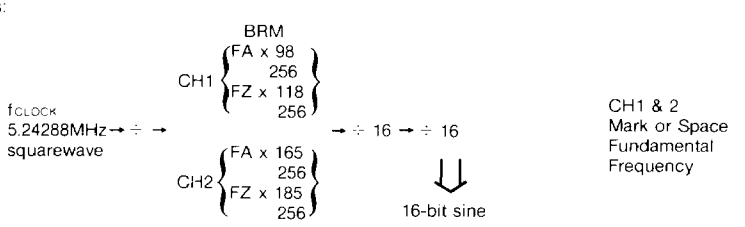
f_{CLOCK} = 5.24288MHz

Parameter	Conditions	Frequency (Hz)
CH1 Mark FZ	Pins 13,14 = 0V	1650
CH1 Space FA	Pin 13 = 0V Pin 14 = 5V	1850
CH2 Mark FZ	Pin 13 = 5V Pin 14 = 0V	980
CH2 Space FA	Pins 13,14 = 5V	1180
Receiver characteristics		
Centre frequency CH1		1080
Lock range CH1		398
Centre frequency CH2		1750
Lock range CH2		335

CIRCUIT DESCRIPTION

The MV9009 forms a digital transmitter and 2nd order PLL for modulation/demodulation of 300 Baud FSK signals. The chip transmits on one channel and receives on the other as defined by the truth Table 1.

The transmitter works by dividing a 5.24288MHz crystal clock as follows:



Baseband shaping is also provided for the data signal, to reduce out of band modulation products. This is performed digitally by taking 8 steps to change the Binary Rate Multiplier from FA to FZ.

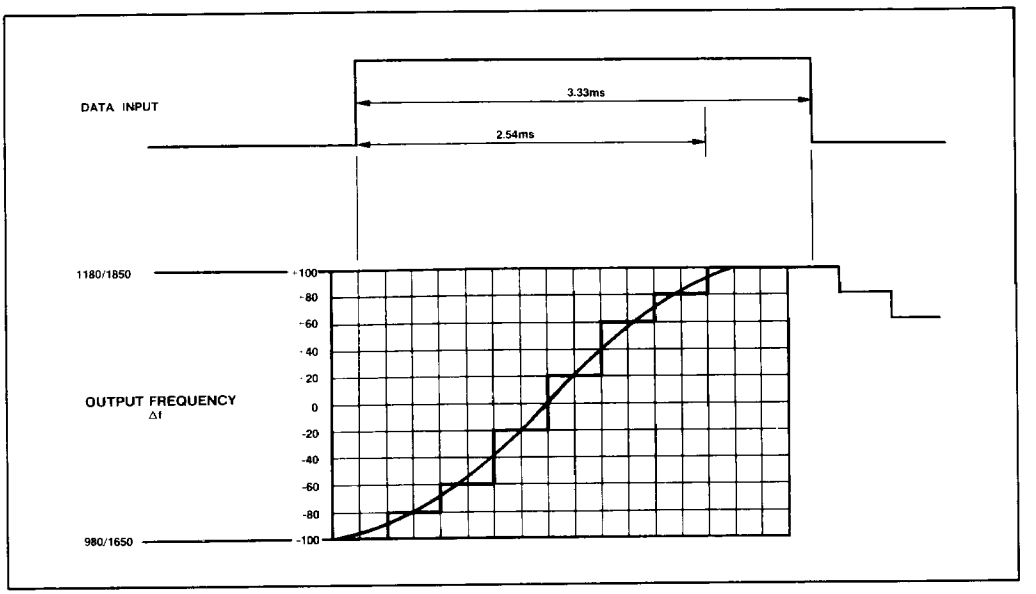


Fig.5

EXAMPLE

If the transmitter is operating at a continuous 980Hz output frequency and the data input goes to '1', the binary rate multiplier output is stepped from x 98/256 to x 118/256 as shown in Fig.5.

The receiver is a 2nd order digital phase locked loop, with an exclusive OR gate phase comparator. CMOS or TTL level FSK inputs are applied to the FSK input pin 16 and the demodulated signal appears at pin 11 as a twice carrier variable mark space ratio signal. A third order low pass post-detection filter and comparator are required in order to produce a data signal. The 2nd order PLL time constants have been optimised to give minimum jitter at 300 baud. Due to finite load times in the 12-bit counters a small amount of bias distortion (0.5%) occurs in the demodulated signal, due to the loss of 1 or 2 least significant bits in the counters.

Fig.7 shows the block diagram for a complete modem also using the SL9009 Adaptive Cancellation Filter.

CHIP TRUTH TABLE

'1' = +5V '0' = 0V

Channel Select Pin 13	Data IN 14	Data Clamp 15	FSK In 16	Transmitter Outputs 1 to 7	PLL Out 11	Lock Detect 12
0	0	0	980Hz 1180Hz	1650Hz	0 1	0
0	1	0	980Hz 1180Hz	1850Hz	0 1	0
1	0	0	1650Hz 1850Hz	980Hz	0 1	0
1	1	0	1650Hz 1850Hz	1180Hz	0 1	0
X	X	1	Valid input signal	S1-S4 0 S5-S7 OFF	PLL still demodulating	0
0	X	X	Inside Lock range	X	Undefined	1
1	X	X	Outside 970-1190Hz and 1640-1860Hz	X	Undefined	1
0	X	X	Outside Lock range	X	Undefined	Mainly 1
1	X	X	Outside	X	Undefined	Mainly 1

NOTE
The lock detector is mainly '1' when the input signal is outside the lock range. If a continuous signal is required a timer circuit is required to time out '0' intervals. Fig.6 shows a suggested circuit.

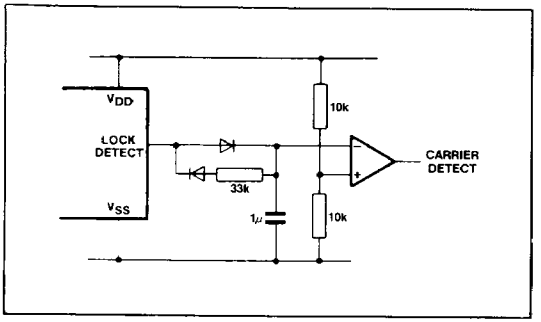


Fig.6

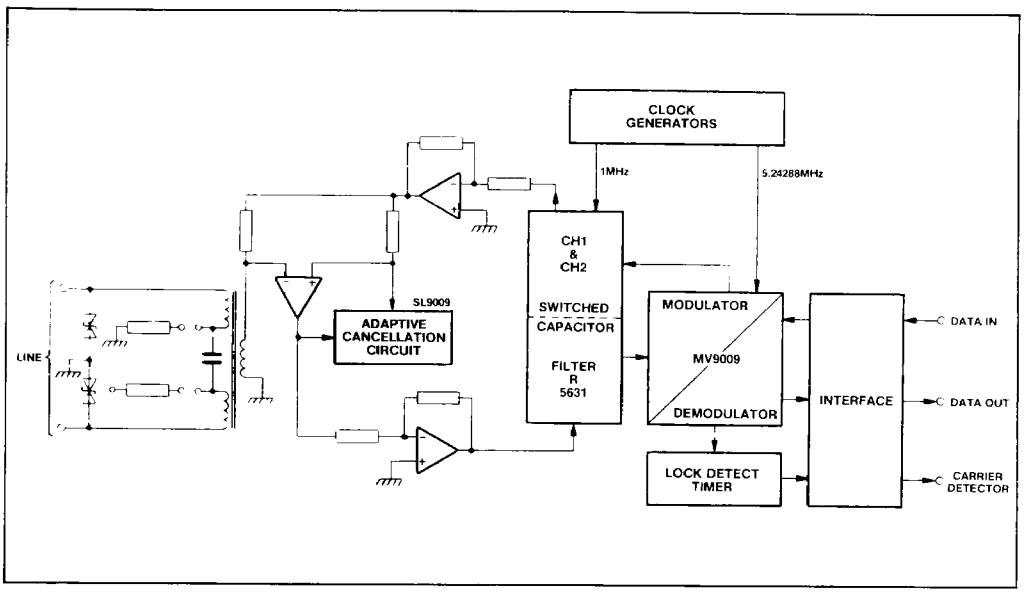


Fig.7 System block diagram

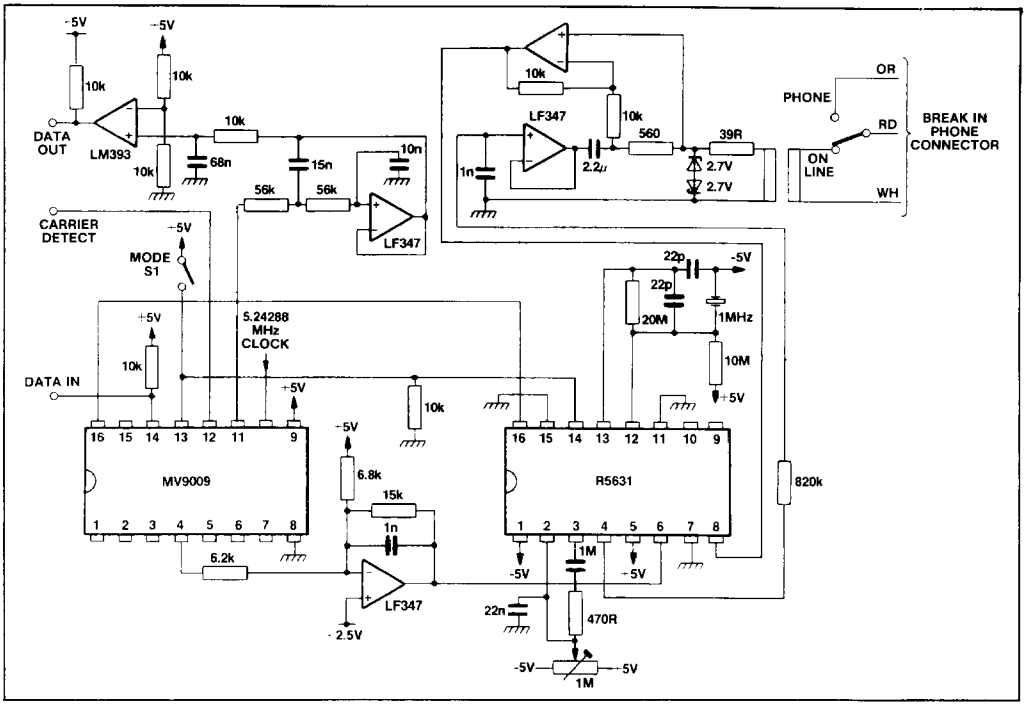


Fig.8 Basic V21 modem