

M52780-XXXSP

I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

DESCRIPTION

M52780 - XXXSP is the I2C BUS controlled Semiconductor Integrated Circuit with 150MHz range 3ch Amp and Letter Indication Controller which function in range 30MHz~80MHz.

VIDEO Pre-Amp includes ,in each channel , Retrace Blanking, Wide Range Amp,Brightness Control,and Bus Controlled Main Sub Contrast ,OSD Adjust Control,5ch D/A Output,and OSD Controller.

Letter Indicate Controller can indicate Characters,such as Chinese character , Hiragana letter , Katakana letter ,English letter , Number letter , and so on. Therefore it is the most suitable for High Resolution Display Monitor.

FEATURES

[Pre - Amp]

- Frequency Band Width:RGB ----- 150 MHz
- Input :RGB ----- 0.7 Vp-p(Typ)
:Retrace BLK ----- 3.0 Vp-p minimum(Positive)
- Output :RGB ----- 4.5 Vp-p(Max)
:OSD ----- 4.5 Vp-p(Max)
- Contrast Control includes Main Control which change 3ch at the same time and Sub Control which change each channel independently. OSD Adjust has Main Control only.
- Both can be controlled by I2C BUS.
- Include Internal and External Pedestal Clamp Circuit.

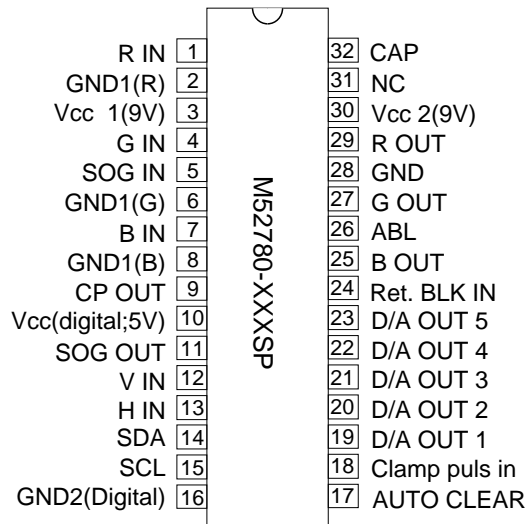
[D/A]

- Output ----- 0 ~ 5V (5ch)

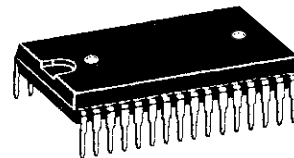
[OSD Controller]

- Screen composition ----- 24 letters x 12 lines
- Number of characters displayed ----- Max 288 letters
- Character composition ----- 12 x 18 dots
- Characters available ----- 256 kinds
- Character sizes available ----- 4(vertical)x 4(horizontal)
- Display locations available
Horizontal direction ----- 1000 locations
Vertical direction ----- 1023 locations
- Blinking Character units
Cycle : division of vertical synchronization signal into 64 or 32
Duty : 25%, 50%, or 75%
- Coloring
Character color ----- Character units
Background coloring ----- Character units
Matrix-outline(shadow)coloring ----- 8 colors (RGB output)
Specified by register
Border coloring ----- 8 colors (RGB output)
Specified by register
Raster coloring ----- 8 colors (RGB output)
Specified by register
- Blanking Blanking off
Character size blanking
Border size blanking
Matrix-outline size blanking
All blanking(all raster area)
- Display RAM erase function
- Display input frequency range ----- 30MHz~80MHz

PIN CONFIGURATION



PACKAGE:32P4B



32 pin plastic SDIP

APPLICATION

CRT DISPLAY MONITOR

RECOMMENDED OPERATING CONDITIONS

- Supply Voltage Range ----- 8.5~9.5V(Analog Part)
4.75~5.25V(Logic Part)
- Rated Supply Voltage ----- 9.0V(Analog Part)
5.0V (Logic Part)

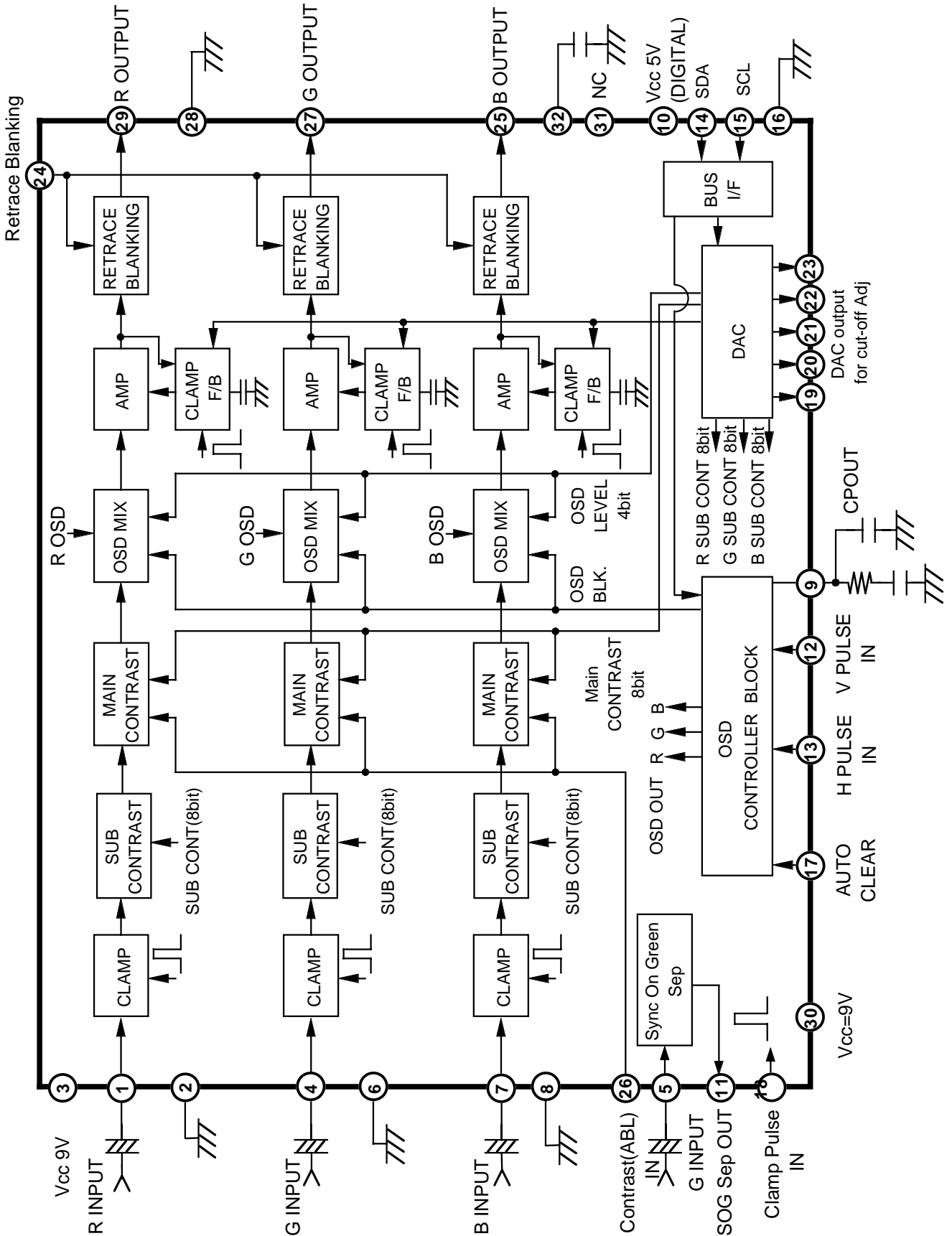
MAJOR SPECIFICATION

I2C BUS Controlled 3ch Video Pre-Amp with OSD Controller

M52780-XXXSP

12C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

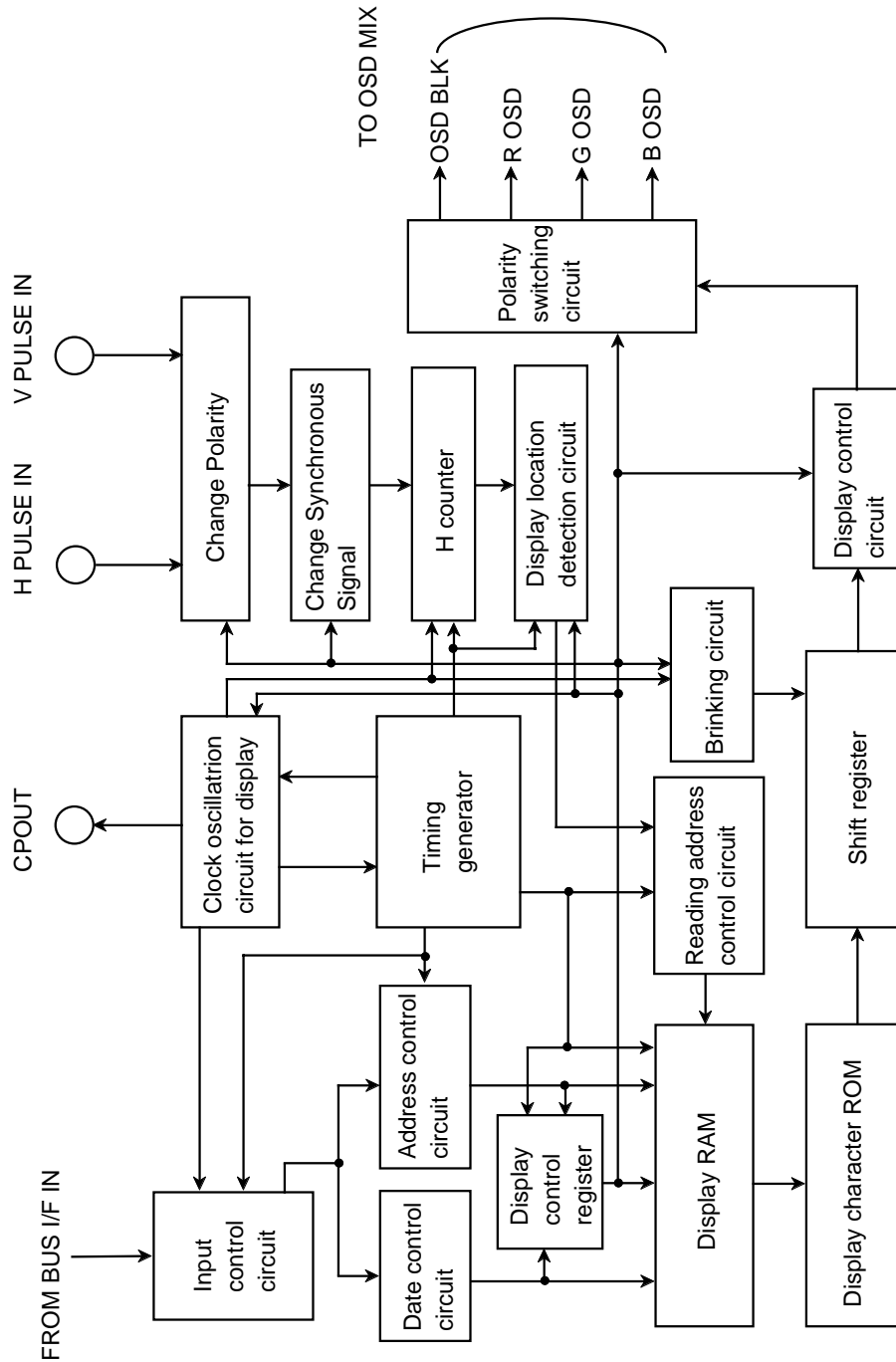
Block Diagram



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OSD CONTROLLER BLOCK



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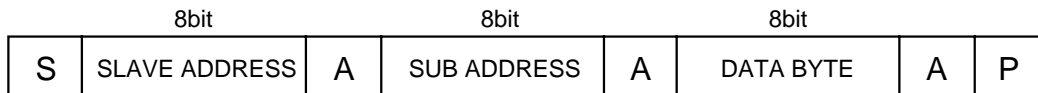
I2C-BUS PROTOCOL

Slave address

	D7	D6	D5	D4	D3	D2	D1	R/W	
VIDEO PRE-AMP	1	0	0	0	1	0	0	0	=88H
OSD CONTROLLER	0	1	1	1	1	1	0	0	=7CH

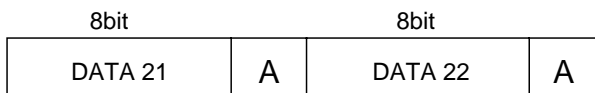
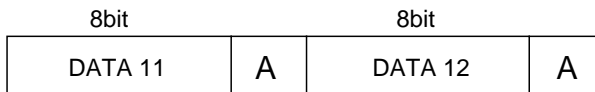
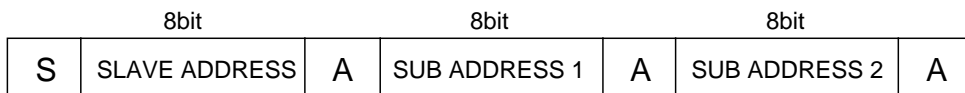
Data transmission format

- Pre - Amp part



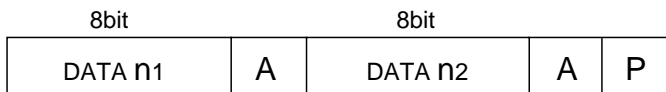
Transmit all data by a timing of Vsync

- OSD part



⋮

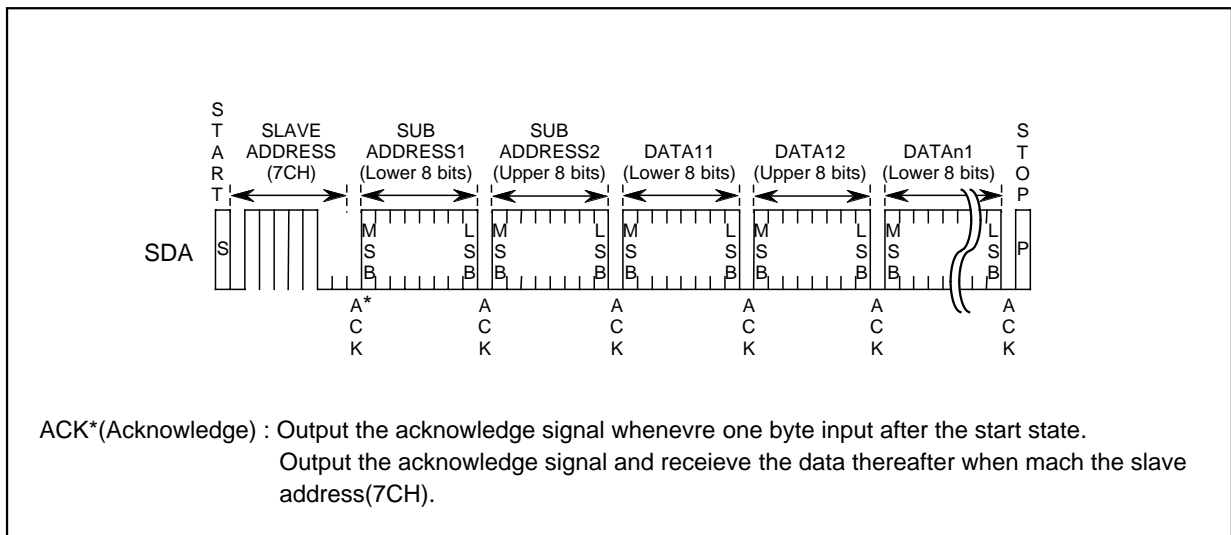
2 bytes after Slave Address set with sub address,
and the address increases by 2 bytes.
Therefore, I don't need to input an address from next data



S : Start condition
A : Acknowledge
P : Stop condition

OSD part data input (Sequence)

- (a) Sub addresses are consists of 16 bits.
- (b) Data is consists of 16 bits.
- (c) Sub addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.
- (d) After the start state has been attained and the control byte (7CH) received, the next 16 bits (2bytes) are for inputting the address. Addresses are increased in increments for every 16 bits (2 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

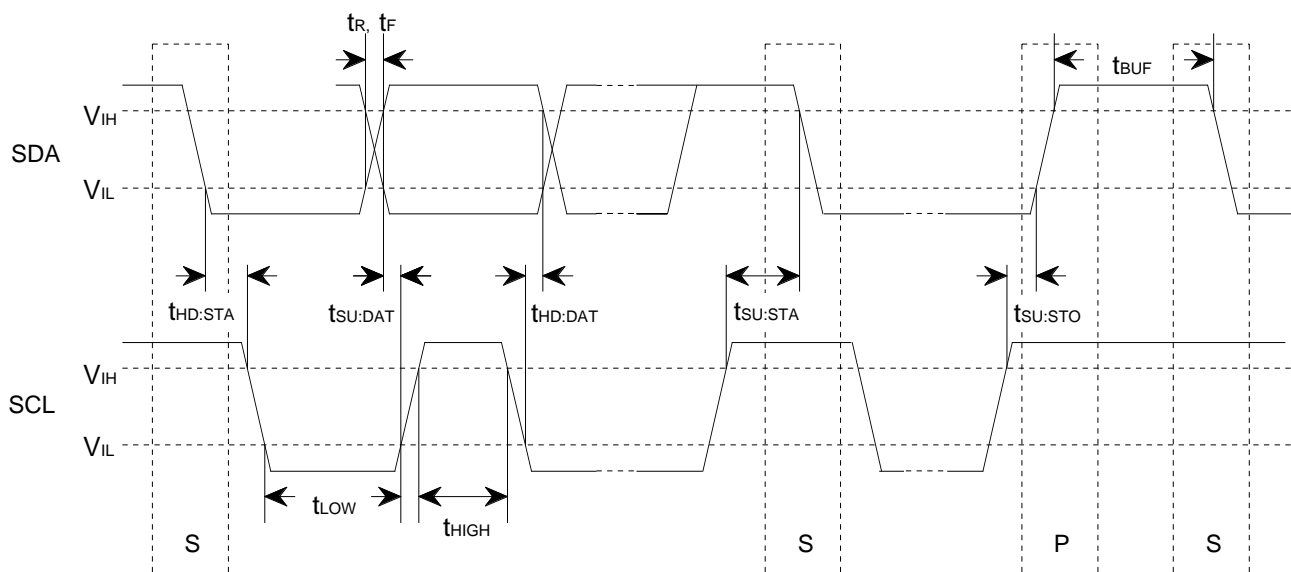


ACK*(Acknowledge) : Output the acknowledge signal whenever one byte input after the start state.
 Output the acknowledge signal and receive the data thereafter when mach the slave address(7CH).

Data input sequence

Timing requirement of I2C

parameter	symbol	MIN	MAX	units
Input voltage LOW	V_{IL}	-0.5	1.5	V
Input voltage HIGH	V_{IH}	3.0	5.5	V
SCL clock frequency	f_{SCL}	0	100	KHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	μs
Hold time start condition.After this period the first clock pulse is generated	$t_{HD:STA}$	4.0	-	μs
The LOW period of the clock	t_{LOW}	4.7	-	μs
The HIGH period of the clock	t_{HIGH}	4.0	-	μs
Set up time for start condition(Only relevant for a repeated start condition)	$t_{SU:STA}$	4.7	-	μs
Hold time for I2C devices	$t_{HD:DAT}$	0	-	μs
Set-up time DATA	$t_{SU:DAT}$	250	-	ns
Rise time of both SDA and SCL	t_R	-	1000	ns
Fall time of both SDA and SCL	t_F	-	300	ns
Set-up time for stop condition	$t_{SU:STO}$	4.0	-	μs



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Pre - Amp Block sub address byte and data byte format

NO.	function	bit	sub add.	Data Byte (top:byte format under:start condition)							
				D7	D6	D5	D4	D3	D2	D1	D0
1	Main contrast	8	00H	A07	A06	A05	A04	A03	A02	A01	A00
				0	1	0	0	0	0	0	0
2	Sub contrast R	8	01H	A17	A16	A15	A14	A13	A12	A11	A10
				1	0	0	0	0	0	0	0
3	Sub contrast G	8	02H	A27	A26	A25	A24	A23	A22	A21	A20
				1	0	0	0	0	0	0	0
4	Sub contrast B	8	03H	A37	A36	A35	A34	A33	A32	A31	A30
				1	0	0	0	0	0	0	0
5	Brightness cont.	8	04H	A47	A46	A45	A44	A43	A42	A41	A40
				1	0	0	0	0	0	0	0
6	OSD level	4	05H	-	-	-	-	A53	A52	A51	A50
				0	0	0	0	1	0	0	0
7	RE-BLK Adjust	4	06H	-	-	-	-	A63	A62	A61	A60
				0	0	0	0	1	0	0	0
8	D/A OUT1	8	07H	A77	A76	A75	A74	A73	A72	A71	A70
				1	0	0	0	0	0	0	0
9	D/A OUT2	8	08H	A87	A86	A85	A84	A83	A82	A81	A80
				1	0	0	0	0	0	0	0
10	D/A OUT3	8	09H	A97	A96	A95	A94	A93	A92	A91	A90
				1	0	0	0	0	0	0	0
11	D/A OUT4	8	0AH	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
				1	0	0	0	0	0	0	0
12	D/A OUT5	8	0BH	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
				1	0	0	0	0	0	0	0

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Electrical Characteristics (Vcc = 9V,5V; Ta = 25°C unless otherwise specified)

No	parameter	Symbol	Test Point(s)	Input						Control voltage	BUS CTL (H)												Standard		Re-mark							
				①④⑦ RGB In	⑤ SOG In	⑫ H In	⑬ V In	⑭ CP In	⑮ Ret BLK		00H Main cont	01H Sub cont 1	02H Sub cont 2	03H Sub cont 3	04H Bright	05H OSD Adj	06H BLK Adj	07H D/A OUT1	08H D/A OUT2	09H D/A OUT3	10AH D/A INT. EXT	MIN	TYP	MAX		Unit						
1	Circuit current1	Icc1	Ia	a	a	a	a	a	a	a	a	5.0	FFH 255	FFH 255	FFH 255	FFH 127	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	00H 0	110	130	mA	Note1 brightness=4V
2	Circuit current2	Icc2	Ib	a	a	a	a	a	a	a	a	5.0	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note2
3	Output dynamic range	Vomax	OUT	b SG2	a	a	a	a	a	a	a	5.0	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note3	
4	Maximum input	Vimax	IN OUT	b SG2 Variable	a	a	a	a	a	a	a	5.0	64H 100	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note4 brightness=1.5V	
5	Maximum gain	Gv	OUT	b SG1	a	a	a	a	a	a	a	5.0	FFH 255	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note5	
6	Relative maximum gain	Gv	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Note6		
7	Main contrast control characteristics 1	VC1	OUT	b SG1	a	a	a	a	a	a	a	5.0	C8H 200	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note7	
8	Main contrast control relative characteristics 1	VC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Note8		
9	Main contrast control characteristics 2	VC2	OUT	b SG1	a	a	a	a	a	a	a	5.0	64H 100	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note9	
10	Main contrast control relative characteristics 2	VC2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Note10		
11	Main contrast control characteristics 3	VC3	OUT	b SG1	a	a	a	a	a	a	a	5.0	14H 20	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note11	
12	Main contrast control relative characteristics 3	VC3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Note12		
13	Sub contrast control characteristics 1	VSC1	OUT	b SG1	a	a	a	a	a	a	a	5.0	FFH 255	C8H 200	C8H 200	C8H 200	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note13	
14	Sub contrast control relative characteristics 1	VSC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Note14		
15	Sub contrast control characteristics 2	VSC2	OUT	b SG1	a	a	a	a	a	a	a	5.0	FFH 255	64H 100	64H 100	64H 100	→	→	→	→	→	→	→	→	→	→	→	→	→	→	Note15	
16	Sub contrast control relative characteristics 2	VSC2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Note16		

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No	parameter	Symbol	Test Point(s)	Input						Control voltage	BUS CTL (H)												Standard		Re-mark	
				①④⑦ RGB In	⑤ SOG In	⑫ H In	⑬ V In	⑭ CP In	⑮ Ret BLK		ABL	00H Main cont	01H Sub cont 1	02H Sub cont 2	03H Sub cont 3	04H Bright Adj	05H OSD Adj	06H BLK Adj	07H D/A OUT1	08H D/A OUT2	09H D/A OUT3	0AH D/A OUT4	0BH INT EXT	MIN		TYP
17	Sub contrast control characteristics 2	VSC3	OUT	b SG1	a	a	a	b SG5	a	5.0	FFH 255	14H 20	14H 20	14H 20	14H 20	3FH 63	00H 0	FFH 255	FFH 255	FFH 255	00H 0	0.8	1.1	1.4	Vp-p	Note17
18	Sub contrast control relative characteristics 2	VSC3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0.8	1.0	1.2	-	Note18	
19	Main/sub contrast control characteristics 2	VMSC	OUT	b SG1	a	a	a	b SG5	a	5.0	C8H 200	C8H 200	C8H 200	C8H 200	-	-	-	-	-	-	2.3	2.9	3.5	Vp-p	Note19	
20	Main/sub contrast control relative characteristics 2	VMSC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0.8	1.0	1.2	-	Note20	
21	ABL control characteristics 1	ABL1	OUT	b SG1	a	a	a	b SG5	a	4.0	FFH 255	FFH 255	FFH 255	FFH 255	-	-	-	-	-	-	3.2	4.0	4.8	Vp-p	Note21	
22	ABL control relative characteristics 1	ABL1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0.8	1.0	1.2	-	Note22	
23	ABL control characteristics 2	ABL2	OUT	b SG1	a	a	a	b SG5	a	2.0	-	-	-	-	-	-	-	-	-	-	1.5	2.0	2.5	Vp-p	Note23	
24	ABL control relative characteristics 2	ABL2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0.8	1.0	1.2	-	Note24	
25	Brightness control characteristics 1	VB1	OUT	a	a	a	a	b SG5	a	5.0	-	-	-	-	7FH 127	-	-	-	-	-	3.3	3.7	4.1	V	Note25	
26	Brightness control relative characteristics 1	VB1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-0.3	0	0.3	V	Note26	
27	Brightness control characteristics 2	VB2	OUT	a	a	a	a	b SG5	a	5.0	-	-	-	-	3FH 63	-	-	-	-	-	1.5	1.8	2.1	V	Note27	
28	Brightness control relative characteristics 2	VB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-0.3	0	0.3	V	Note28	
29	Brightness control characteristics 3	VB3	OUT	a	a	a	a	b SG5	a	5.0	-	-	-	-	1FH 31	-	-	-	-	-	0.7	0.9	1.1	V	Note29	
30	Brightness control relative characteristics 3	VB3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-0.3	0	0.3	V	Note30	
31	Frequency characteristics 1 (f=50MHz)	FC1	OUT	b SG3	a	a	a	a 5V	a	5.0	Variable	-	-	-	Variable	-	-	-	-	-	-2.0	0	2.5	dB	Note31	
32	Frequency relative characteristics 1 (f=50MHz)	FC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-1.0	0	1.0	dB	Note32	

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33	Frequency characteristics 1 (f=150MHz)	FC1'	OUT	b SG3	a	a	a	a	a	a	a	5.0	Variable	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	0	3.0	dB	Note33	
34	Frequency relative characteristics 1 (f=150MHz)	FC1'	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	dB	Note34
35	Frequency characteristics 2 (f=150MHz)	FC2	OUT	b SG3	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	3.0	5.0	dB	Note35	
36	Frequency relative characteristics 2 (f=150MHz)	FC2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	dB	Note36
37	Crosstalk 1 (f=50MHz)	CT1	OUT(29) OUT(32)	2b SG3 6a 11a	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	-25	-20	dB	Note37	
38	Crosstalk 1 (f=150MHz)	CT1'	OUT(29) OUT(32)	2b SG3 6a 11a	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	-15	-10	dB	Note38	
39	Crosstalk 2 (f=50MHz)	CT2	OUT(29) OUT(35)	2a 6b SG3 11a	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	-25	-20	dB	Note39	
40	Crosstalk 2 (f=150MHz)	CT2'	OUT(29) OUT(35)	2a 6b SG3 11a	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	-15	-10	dB	Note40	
41	Crosstalk 3 (f=50MHz)	CT3	OUT(32) OUT(35)	2a 6a 11b SG3	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	-25	-20	dB	Note41	
42	Crosstalk 3 (f=150MHz)	CT3'	OUT(32) OUT(35)	2a 6a 11b SG3	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	-15	-10	dB	Note42	
43	Pulse characteristics 1 (4VP-P)	Tr	OUT	b SG1	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	1.7	-	nS	Note43	
44	Pulse characteristics 2 (4VP-P)	Tf	OUT	b SG1	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	3.0	-	nS	Note44	
45	Clamp pulse threshold voltage	VthCP	OUT	b SG1	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	1.5	2.0	V	Note45	
46	Clamp pulse minimum width	WCP	OUT	b SG1	a	a	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	0.5	-	μS	Note46	
47	OSD pulse characteristics 1	OTr	OUT	a	a	b SG6	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	3.0	6.0	nS	Note47	
48	OSD pulse characteristics 2	OTf	OUT	a	a	b SG6	a	a	a	a	a	5.0	a	5.0	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	FFH 255	0	3.0	6.0	nS	Note48	

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Note 1) Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IA.

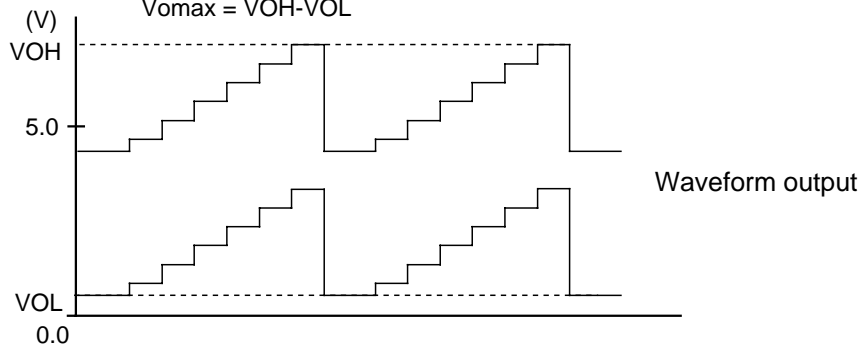
Note 2) Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IB.

Note 3) Decrease V30 gradually, and measure the voltage when the waveform output is distorted. The voltage is called VOL.

Next, increase V30 gradually, and measure the voltage when the top of waveform output is distorted. The voltage is called VOH.

Voltage Vomax is calculated by the equation below:

$$V_{omax} = VOH - VOL$$



Note 4) Increase the input signal (SG2) amplitude gradually, starting from 700mVp-p. Measure the amplitude of the input signal when the output signal starts becoming distorted.

Note 5) Input SG1, and read the amplitude output at OUT(29,32,35). The amplitude is called VOUT(29,32,35). Maximum gain GV is calculated by the equation below:

$$GV = 20 \log(VOUT/0.7) \text{ (dB)}$$

Note 6) Relative maximum gain GV is calculated by the equation below:

$$GV = \frac{VOUT(29)}{VOUT(32)}, \\ \frac{VOUT(32)}{VOUT(35)}, \\ \frac{VOUT(35)}{VOUT(29)}$$

Note 7) Measuring the amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35). Main contrast control characteristics VC1 is calculated by the equation below:

$$VC1 = 20 \log(VOUT/0.7) \text{ (dB)}$$

Note 8) Relative characteristics VC1 is calculated by the equation below:

$$VC1 = \frac{VOUT(29)}{VOUT(32)}, \\ \frac{VOUT(32)}{VOUT(35)}, \\ \frac{VOUT(35)}{VOUT(29)}$$

Note 9) Measuring condition and procedure are the same as described in Note 7.

Note 10) Measuring condition and procedure are the same as described in Note 8.

Note 11) Measuring condition and procedure are the same as described in Note 7.

Note 12) Measuring condition and procedure are the same as described in Note 8.

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Note 13) Measure the amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35). Sub contrast control characteristics VSC1 is calculated by the equation below:

$$VSC1=20\text{Log}(VOUT/0.7) \text{ (dB)}$$

Note 14) Relative characteristics VSC1 is calculated by the equation below:

$$VCS1=VOUT(29)/VOUT(32), \\ VOUT(32)/VOUT(35), \\ VOUT(35)/VOUT(29).$$

Note 15) Measuring condition and procedure are the same as described in Note13.

Note 16) Measuring condition and procedure are the same as described in Note14.

Note 17) Measuring condition and procedure are the same as described in Note13.

Note 18) Measuring condition and procedure are the same as described in Note14.

Note 19) Measure the amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35). Main/Sub contrast control characteristics VMSC is calculated by the equation below:

$$VMSC=20\text{log}(VOUT/0.7) \text{ (dB)}$$

Note 20) Relative characteristics VMSC is calculated by the equation below:

$$VMSC=VOUT(29)/VOUT(32) , \\ VOUT(32)/VOUT(35) , \\ VOUT(35)/VOUT(29)$$

Note 21) Measure the amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35), and is treated as ABL1.

Note 22) Relative characteristics ABL1 is calculated by the equation below:

$$ABL1=VOUT(29)/VOUT(32) , \\ VOUT(32)/VOUT(35) , \\ VOUT(35)/VOUT(29)$$

Note 23) Measuring condition and procedure are the same as described in Note21.

Note 24) Measuring condition and procedure are the same as described in Note22.

Note 25) Measure the DC voltage at OUT(29,32,35) with a voltmeter. The measured value is called VOUT(29,32,35), and is treated as VB1.

Note 26) Relative characteristics VB1 is calculated by the difference in the output between the channels.

$$VB1=VOUT(29)-VOUT(32) , \\ VOUT(32)-VOUT(35) , \\ VOUT(35)-VOUT(29)$$

Note 27) Measuring condition and procedure are the same as described in Note25.

Note 28) Measuring condition and procedure are the same as described in Note26.

Note 29) Measuring condition and procedure are the same as described in Note25.

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- Note 30) Measuring condition and procedure are the same as described in Note26.
- Note 31) First, SG3 to 1MHz is as input signal. Input a resistor that is about 2K to offer the voltage at input pins(2,6,11) in order that the bottom of input signal is 2.5V. Control the main contrast in order that the amplitude of sine wave output is 4.0Vp-p. Control the brightness in order that the bottom of sine wave output is 2.0Vp-p. By the same way, measure the output amplitude when SG3 to 50MHz is as input signal. The measured value is called VOUT(29,32,35). Frequency characteristics FC1(29,32,35) is calculated by the equation below:

$$FC1=20 \log[VOUT(Vp-p)/\text{output amplitude when inputted SG3(1MHz):4Vp-p}](dB)$$
- Note 32) Relative characteristics FC1 is calculated by the difference in the output between the channels.
- Note 33) Measuring condition and procedure are the same as described in Note31, expect SG3 to 150MHz.
- Note 34) Relative characteristics FC1' is calculated by the difference in the output between the channels.
- Note 35) SG3 to 1MHz is as input signal. Control the main contrast in order that the amplitude of sine wave output is 1.0Vp-p. By the same way, measure the output amplitude when SG3 to 150MHz is as input signal. The measured value is called VOUT(29,32,35). Frequency characteristics FC2(29,32,35) is calculated by the equation below:

$$FC1=20 \log[VOUT(Vp-p)/\text{output amplitude when inputted SG3(1MHz):4Vp-p}](dB)$$
- Note 36) Relative characteristics FC2 is calculated by the difference in the output between the channels.
- Note 37) Input SG3 (50MHz) to pin2 only, and then measure the waveform amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35). Crosstalk CT1 is calculated by the equation below:

$$CT1=20 \log [VOUT(29,32)/VOUT(35)] \text{ (dB)}$$
- Note 38) Measuring condition and procedure are the same as described in Note37, expect SG3 to 150MHz.
- Note 39) Input SG3 (50MHz) to pin6 only, and then measure the waveform amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35). Crosstalk CT2 is calculated by the equation below:

$$CT2=20 \log [VOUT(29,35)/VOUT(32)] \text{ (dB)}$$
- Note 40) Measuring condition and procedure are the same as described in Note39, expect SG3 to 150MHz.
- Note 41) Input SG3 (50MHz) to pin11 only, and then measure the waveform amplitude output at OUT(29,32,35). The measured value is called VOUT(29,32,35). Crosstalk CT2 is calculated by the equation below:

$$CT3=20 \log [VOUT(32,35)/VOUT(29)] \text{ (dB)}$$
- Note 42) Measuring condition and procedure are the same as described in Note41, expect SG3 to 150MHz.
- Note 43) Control the main contrast (00H) in order that the amplitude of output signal is 4.0Vp-p. Control the brightness (V30) in order that the Black level of output signal is 2.0V. Measure the time needed for the input pulse to rise from 10 % to 90 % (Tr1) and for the output pulse to rise from 10 % to 90 % (Tr2) with an active probe. Pulse characteristics Tr is calculated by the equations below :

$$Tr = \sqrt{[(Tr2)^2 - (Tr1)^2]} \text{ (nsec)}$$

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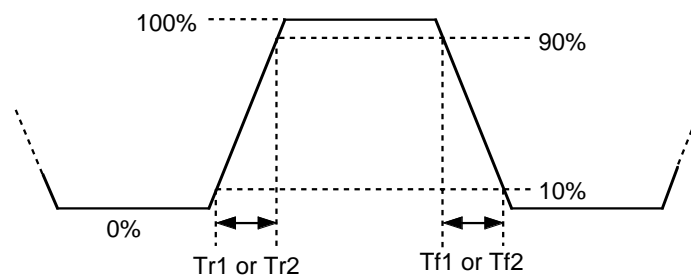
Note 43a) Relative characteristics Tr is calculated by the difference in the output between the channels.

Note 44) Measure the time needed for the input pulse to fall from 90 % to 10 % ($Tf1$) and for the output pulse to fall from 90 % to 10 % ($Tf2$) with an active prove.

Pulse characteristics Tf is calculated by the equations below :

$$Tf = \sqrt{[(Tf2)^2 - (Tf1)^2]} \quad (\text{nsec})$$

Note 44a) Relative characteristics Tf is calculated by the difference in the output between the channels.



Note 45) Turn down the SG5 input level gradually from 5.0Vp-p, monitoring the waveform output. Measure the top level of input pulse when the output pedestal voltage turn decrease with unstable.

Note 46) Decrease the SG5 pulse width gradually from 0.5 μ s, monitoring the output. Measure the SG5 pulse width (a point of 1.5V) when the output pedestal voltage turn decrease with unstable.

Note 47) Measure the time needed for the output pulse to rise from 10% to 90% (OTr) with an active prove.

Note 48) Measure the time needed for the output pulse to fall from 90% to 10% (OTf) with an active prove.

Note 49) Measure the amplitude output at OUT(29,32,35). The measured value is called $VOUT(29,32,35)$, and is treated as $Oaj1$.

Note 50) Relative characteristics $Oaj1$ is calculated by the equation below:

$$Oaj1 = \frac{VOUT(29)}{VOUT(32)}, \\ \frac{VOUT(32)}{VOUT(35)}, \\ \frac{VOUT(35)}{VOUT(29)}$$

Note 51) Measuring condition and procedure are the same as described in Note49.

Note 52) Measuring condition and procedure are the same as described in Note50.

Note 53) Measuring condition and procedure are the same as described in Note49.

Note 54) Measuring condition and procedure are the same as described in Note50.

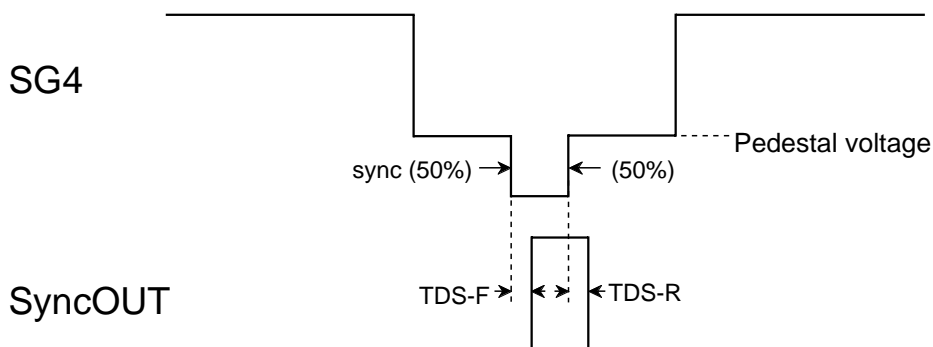
Note 55) Measure the amplitude output is blanked by the SG6at OUT(29,32,35). The measured value is called $VOUT(29,32,35)$, and is treated as $HBLK1$.

Note 56) Measure the amplitude output is blanked by the SG6at OUT(29,32,35). The measured value is called $VOUT(29,32,35)$, and is treated as $HBLK2$.

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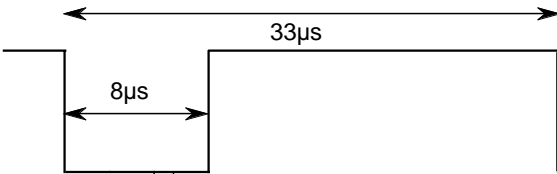
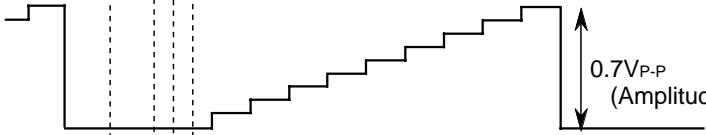
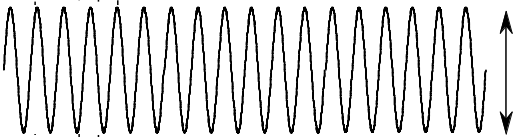
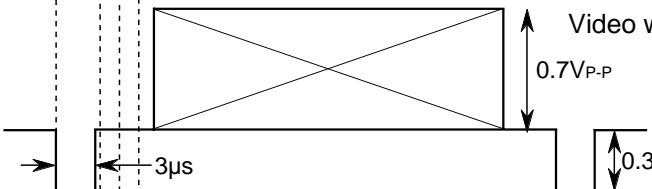


- Note 57) Measure the amplitude output is blanked by the SG6at OUT(29,32,35). The measured value is called VOUT(29,32,35), and is treated as HBLK3.
- Note 58) Confirm that output signal is being blanked by the SG6at the time.
Monitoring to output signal, decreasing the level of SG6. Measure the top level of SG6 when the blanking period is disappeared. The measured value is called VthRET.
- Note 59) The sync's amplitude of SG4 be changed all white into all black, increase from 0Vp-p to 0.02Vp-p.
No pulse output permitted.
- Note 60) The sync's amplitude of SG4 be changed all white or all black, decrease from 0.3Vp-p to 0.2Vp-p.
Confirm no malfunction produced by noise.
- Note 61) Measure the high voltage at SyncOUT. The measured value is treated as VSH.
- Note 62) Measure the low voltage at SyncOUT. The measured value is treated as VSL.
- Note 63) SyncOUT becomes High with sync part of SG4.
Measure the time needed for the rear edge of SG4 sync to fall from 50 % and for SyncOUT to rise from 50 % with an active prove. The measured value is treated as TDS-F ,less than 90nsec.
- Note 64) Measure the time needed for the rear edge of SG4 sync to rise from 50 % and for SyncOUT to fall from 50 % with an active prove. The measured value is treated as TDS-R ,less than 90nsec.



- Note 65) Measure the DC voltage at D/AOUT. The measured value is treated as VOH.
- Note 66) Measure the DC voltage at D/AOUT. The measured value is treated as VOL.
- Note 67) Electric current flow from the output of D/AOUT must be less than 1.0 mA.
Electric current flow in the output of D/AOUT must be less than 0.4 mA.
- Note 68) The difference of differential non-linearity of D/AOUT must be less than ± 1.0 LSB.

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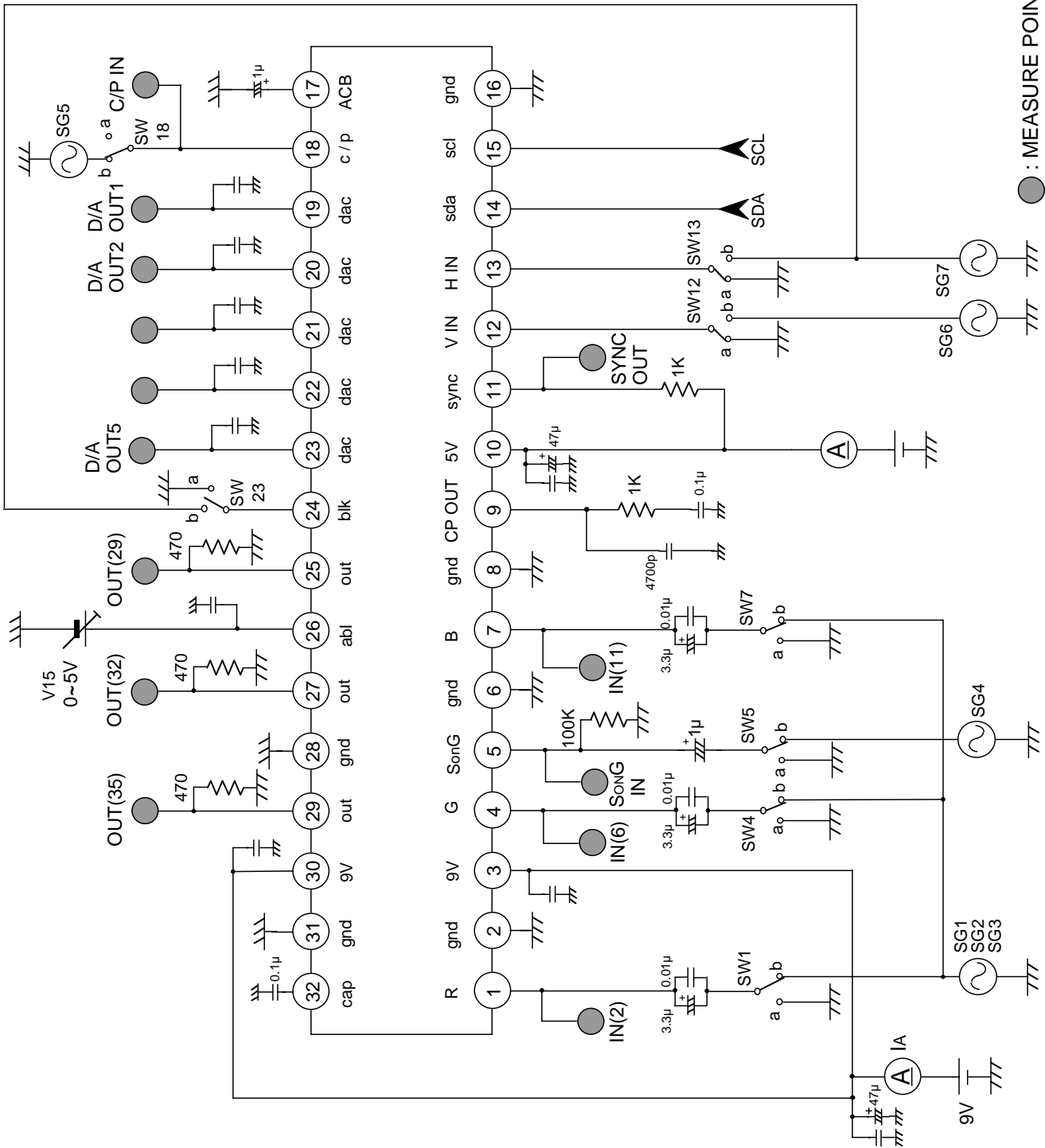
I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

SG No.	INPUT SIGNAL
<p>SG1 Video signal (all white)</p>	 <p>Pulse with amplitude of 0.7Vp-p (f=30KHz). Video width of 25 µs. (75%) 0.7V_{P-P}</p>
<p>SG2 Video signal (step wave)</p>	 <p>0.7V_{P-P} (Amplitude is partially variable.)</p>
<p>SG3 Sine wave (for freq. char.)</p>	 <p>Sine wave amplitude of 0.7Vp-p. f=1MHz,50MHz,150MHz(variable)</p>
<p>SG4 Videosignal (all white,all black)</p>	 <p>Video width of 25µs. (75%) 0.7V_{P-P} all white or all black variable. 3µs 0.3V_{PP} Sync's amplitude is variable.</p>
<p>SG5 Clamp pulse</p>	 <p>0.5µs Pulse width and amplitude are variable. 5V_{TTL}</p>
<p>SG6 BLK pulse</p>	 <p>5µs 5V_{TTL} Amplitude is partially variable.</p>

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TEST CIRCUIT



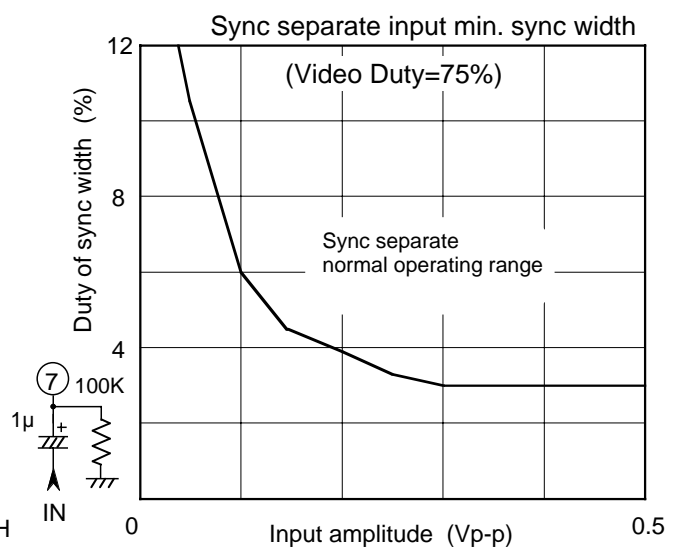
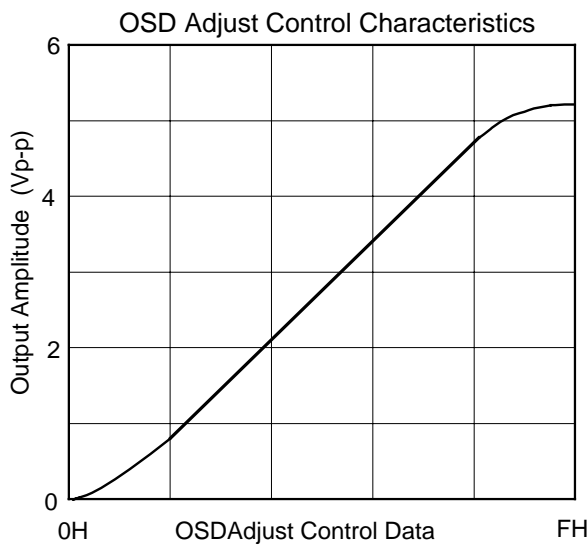
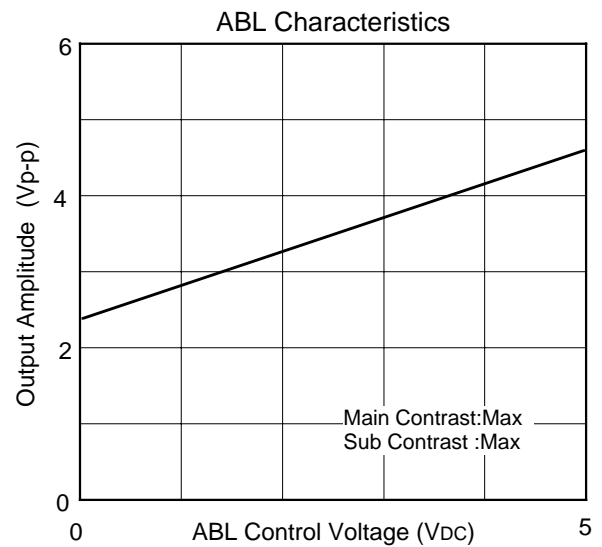
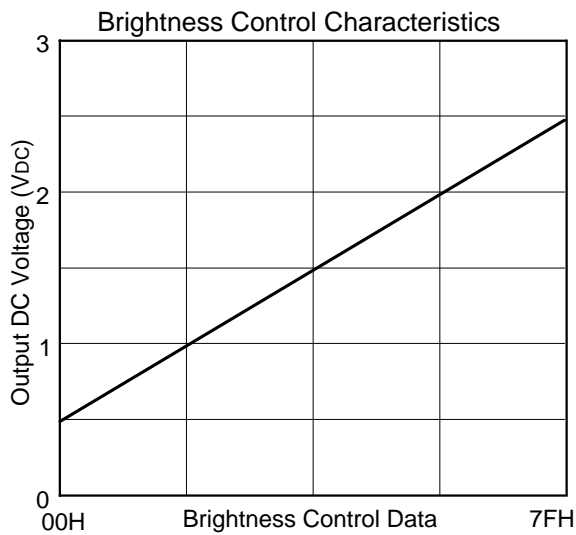
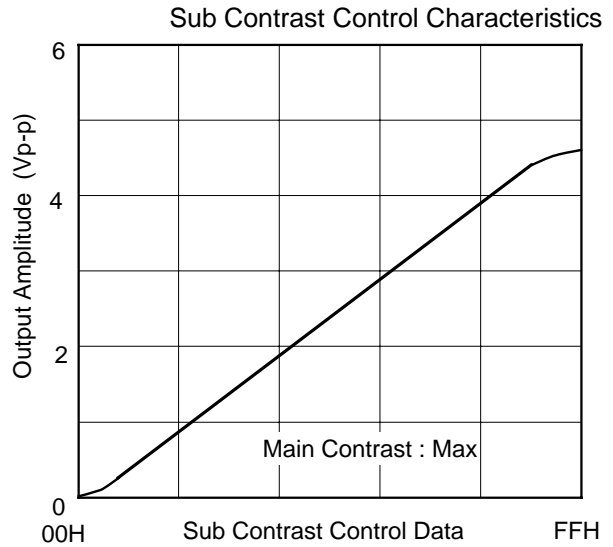
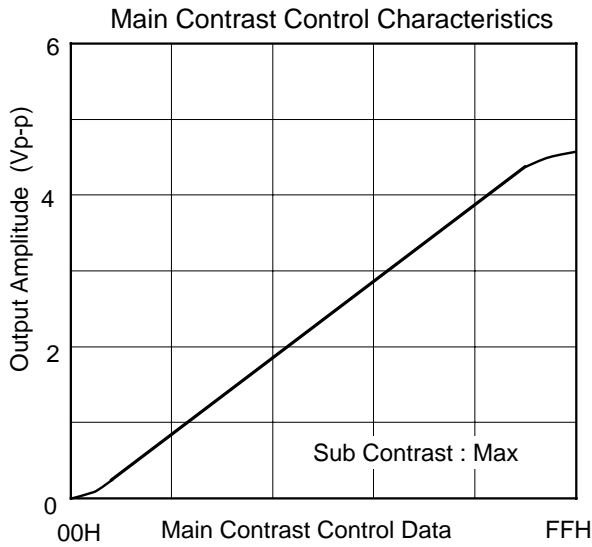
● : MEASURE POINT

* Condenser: 0.01µF (unless otherwise specified.)

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

Typical Characteristics



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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

MEMORY CONSTITUTION

Address 0000_H to 011F_H are assigned to the display RAM, address 0120_H to 0128_H are assigned to the display control registers. The internal circuit is reset and all display control registers (address 0120_H to 0128_H) are set to "0" and display RAM (address 0000_H to 011F_H) are set to "00FF_H" when the \overline{AC} pin level is "L".

Memory constitution is shown in Figure 1.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

Sub address	Upper 8 bits (DATA n2)								Lower 8 bits (DATA n1)							
	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0000 _H	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			⋮	Character color			Character code							
011F _H	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
0120 _H	0	0	DIVS2	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
0121 _H	0	0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
0122 _H	0	0	SPACE2	SPACE1	SPACE0	MOVON	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
0123 _H	0	0	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
0124 _H	0	0	PTC67	MOVE	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
0125 _H	0	0	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
0126 _H	0	0	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
0127 _H	0	0	HSZ21	HSZ20	HSZ11	HSZ10	BETA14	VB	VG	VR	FB	FG	FR	RB	RG	RR
0128 _H	0	0	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/F	BCOL

Memory constitution

Column Rank	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	0000 _H	0001 _H	0002 _H	0003 _H	0004 _H	0005 _H	0006 _H	0007 _H	0008 _H	0009 _H	000A _H	000B _H	000C _H	000D _H	000E _H	000F _H	0010 _H	0011 _H	0012 _H	0013 _H	0014 _H	0015 _H	0016 _H	0017 _H
2	0018 _H	0019 _H	001A _H	001B _H	001C _H	001D _H	001E _H	001F _H	0020 _H	0021 _H	0022 _H	0023 _H	0024 _H	0025 _H	0026 _H	0027 _H	0028 _H	0029 _H	002A _H	002B _H	002C _H	002D _H	002E _H	002F _H
3	0030 _H	0031 _H	0032 _H	0033 _H	0034 _H	0035 _H	0036 _H	0037 _H	0038 _H	0039 _H	003A _H	003B _H	003C _H	003D _H	003E _H	003F _H	0040 _H	0041 _H	0042 _H	0043 _H	0044 _H	0045 _H	0046 _H	0047 _H
4	0048 _H	0049 _H	004A _H	004B _H	004C _H	004D _H	004E _H	004F _H	0050 _H	0051 _H	0052 _H	0053 _H	0054 _H	0055 _H	0056 _H	0057 _H	0058 _H	0059 _H	005A _H	005B _H	005C _H	005D _H	005E _H	005F _H
5	0060 _H	0061 _H	0062 _H	0063 _H	0064 _H	0065 _H	0066 _H	0067 _H	0068 _H	0069 _H	006A _H	006B _H	006C _H	006D _H	006E _H	006F _H	0070 _H	0071 _H	0072 _H	0073 _H	0074 _H	0075 _H	0076 _H	0077 _H
6	0078 _H	0079 _H	007A _H	007B _H	007C _H	007D _H	007E _H	007F _H	0080 _H	0081 _H	0082 _H	0083 _H	0084 _H	0085 _H	0086 _H	0087 _H	0088 _H	0089 _H	008A _H	008B _H	008C _H	008D _H	008E _H	008F _H
7	0090 _H	0091 _H	0092 _H	0093 _H	0094 _H	0095 _H	0096 _H	0097 _H	0098 _H	0099 _H	009A _H	009B _H	009C _H	009D _H	009E _H	009F _H	00A0 _H	00A1 _H	00A2 _H	00A3 _H	00A4 _H	00A5 _H	00A6 _H	00A7 _H
8	00A8 _H	00A9 _H	00AA _H	00AB _H	00AC _H	00AD _H	00AE _H	00AF _H	00B0 _H	00B1 _H	00B2 _H	00B3 _H	00B4 _H	00B5 _H	00B6 _H	00B7 _H	00B8 _H	00B9 _H	00BA _H	00BB _H	00BC _H	00BD _H	00BE _H	00BF _H
9	00C0 _H	00C1 _H	00C2 _H	00C3 _H	00C4 _H	00C5 _H	00C6 _H	00C7 _H	00C8 _H	00C9 _H	00CA _H	00CB _H	00CC _H	00CD _H	00CE _H	00CF _H	00D0 _H	00D1 _H	00D2 _H	00D3 _H	00D4 _H	00D5 _H	00D6 _H	00D7 _H
10	00D8 _H	00D9 _H	00DA _H	00DB _H	00DC _H	00DD _H	00DE _H	00DF _H	00E0 _H	00E1 _H	00E2 _H	00E3 _H	00E4 _H	00E5 _H	00E6 _H	00E7 _H	00E8 _H	00E9 _H	00EA _H	00EB _H	00EC _H	00ED _H	00EE _H	00EF _H
11	00F0 _H	00F1 _H	00F2 _H	00F3 _H	00F4 _H	00F5 _H	00F6 _H	00F7 _H	00F8 _H	00F9 _H	00FA _H	00FB _H	00FC _H	00FD _H	00FE _H	00FF _H	0100 _H	0101 _H	0102 _H	0103 _H	0104 _H	0105 _H	0106 _H	0107 _H
12	0108 _H	0109 _H	010A _H	010B _H	010C _H	010D _H	010E _H	010F _H	0110 _H	0111 _H	0112 _H	0113 _H	0114 _H	0115 _H	0116 _H	0117 _H	0118 _H	0119 _H	011A _H	011B _H	011C _H	011D _H	011E _H	011F _H

The hexadecimal numbers in the boxes show the display RAM address.

Screen constitution

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

REGISTERS DESCRIPTION

(1) Address 0120 H

DA	Register	Contents		Remarks																																		
		Status	Function																																			
0	DIV0	⓪	Set multiply value (frequency value) of horizontal synchronous frequency. $N1 = \sum_{n=0}^{10} (DIV\ n \times 2^n)$ N1:frequency value	Display frequency is computed as show below. $F_{osc} = f_H \times N1$ Fosc [MHz] : Display frequency fH [KHz] : Horizontal synchronous signal frequency to HOR pin. N1 : Shown left Set display frequency Fosc to within 30MHz to 80MHz range. When display frequency Fosc, set frequency value N2 in association with DIVS0 and DIVS1.																																		
		1																																				
1	DIV1	⓪																																				
		1																																				
2	DIV2	⓪																																				
		1																																				
3	DIV3	⓪																																				
		1																																				
4	DIV4	⓪																																				
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5	DIV5	⓪																																				
		1																																				
6	DIV6	⓪																																				
		1																																				
7	DIV7	⓪																																				
		1																																				
8	DIV8	⓪																																				
		1																																				
9	DIV9	⓪																																				
		1																																				
A	DIVS0	⓪																																				
		1																																				
B	DIVS1	⓪			Set frequency value N2 <table border="1" style="margin: 5px 0;"> <thead> <tr> <th colspan="2">DIVS</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Division into 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>Division into 3</td> </tr> <tr> <td>1</td> <td>0</td> <td>Division into 4</td> </tr> <tr> <td>1</td> <td>1</td> <td>Do not set</td> </tr> </tbody> </table>	DIVS							Frequency value N2	1	0		0	0	Division into 2	0	1	Division into 3	1	0	Division into 4	1	1	Do not set	Set frequency value N2 in association with display frequency range. <table border="1" style="margin: 5px 0;"> <thead> <tr> <th>Display frequency</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>55 ~ 80</td> <td>Division into 2</td> </tr> <tr> <td>40 ~ 55</td> <td>Division into 3</td> </tr> <tr> <td>30 ~ 40</td> <td>Division into 4</td> </tr> </tbody> </table>	Display frequency	Frequency value N2	55 ~ 80	Division into 2	40 ~ 55	Division into 3	30 ~ 40	Division into 4	
		DIVS				Frequency value N2																																
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C	DIVS2	⓪																																				
		1																																				
D	DIVS3	⓪			Normally set to "0".																																	
		1					Do not set																															

Note 1 : The mark ⓪ around the status value means the reset status by the "L" level is input to \overline{AC} pin.

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(2) Address 0121 H

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	⓪	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 setting.
		1	BLNK0 output. Polarity is set by PTD0.	
1	PTC1	⓪	P1 output (port P1). Port data is set by PTD1.	
		1	R signal output. Polarity is set by PTD1.	
2	PTC2	⓪	P2 output (port P2). Port data is set by PTD2.	
		1	Do not set.	
3	PTC3	⓪	P3 output (port P3). Port data is set by PTD3.	
		1	G signal output. Polarity is set by PTD3.	
4	PTC4	⓪	P4 output (port P4). Port data is set by PTD4.	
		1	Do not set.	
5	PTC5	⓪	P5 output (port P5). Port data is set by PTD5.	
		1	B signal output. Polarity is set by PTD5.	
6	PTD0	⓪	"L" output (P0 output) or negative polarity output (BLNK0 output).	P0 pin deta control.
		1	"H" output (P0 output) or positive polarity output (BLNK0 output).	
7	PTD1	⓪	"L" output (P1 output) or negative polarity output (R signal output).	P1 pin deta control.
		1	"H" output (P1 output) or positive polarity output (R signal output).	
8	PTD2	⓪	"L" output (P2 output).	Set P2 output level.
		1	"H" output (P2 output).	
9	PTD3	⓪	"L" output (P3 output) or negative polarity output (G signal output).	P3 pin deta control.
		1	"H" output (P3 output) or positive polarity output (G signal output).	
A	PTD4	⓪	"L" output (P4 output).	Set P4 output level.
		1	"H" output (P4 output).	
B	PTD5	⓪	"L" output (P5 output) or negative polarity output (B signal output).	P5 pin deta control.
		1	"H" output (P5 output) or positive polarity output (B signal output).	
C	PTD6	⓪	"L" output (P6 output).	Set P6 output level.
		1	"H" output (P6 output).	
D	PTD7	⓪	"L" output (P7 output).	Set P7 output level.
		1	"H" output (P7 output).	

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(3) Address 0122 H

DA	Register	Contents		Remarks																																											
		Status	Function																																												
0	HP0 (LSB)	⓪	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^9 2^n HP_n + N \right)$ T: The cycle of display frequency	Horizontal display start location is specified using the 10 bits from HP9 to HP0. Note: HP9 to HP0 = (0000000000 ₂) and (000010111 ₂) setting is forbidden																																											
		1																																													
1	HP1	⓪	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>HSZ11</th> <th>HSZ10</th> <th>Frequency value N2</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Division into 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>Division into 3</td> </tr> <tr> <td>1</td> <td>0</td> <td>Division into 4</td> </tr> <tr> <td>1</td> <td>1</td> <td>Do not set</td> </tr> </tbody> </table> 1000 settings are possible		HSZ11	HSZ10	Frequency value N2	0	0	Division into 2	0	1	Division into 3	1	0	Division into 4	1	1	Do not set																												
		HSZ11			HSZ10	Frequency value N2																																									
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0	1	Division into 3																																													
1	0	Division into 4																																													
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3	HP3	⓪																																													
		1																																													
4	HP4	⓪																																													
		1																																													
5	HP5	⓪																																													
		1																																													
6	HP6	⓪																																													
		1																																													
7	HP7	⓪																																													
		1																																													
8	HP8	⓪																																													
		1																																													
9	HP9 (MSB)	⓪																																													
		1																																													
A	TEST9	⓪				Normally set to "0".																																									
		1				Test mode																																									
B	SPACE0	⓪				<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="3">SPACE</th> <th>Number of Lines and Space (□ represents space)</th> </tr> </thead> <tbody> <tr> <td>2</td> <td>1</td> <td>0</td> <td>12</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1 □ 10 □ 1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>2 □ 8 □ 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>3 □ 6 □ 3</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>4 □ 4 □ 4</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>5 □ 2 □ 5</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>6 □ 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6 □ □ 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>6 □ □ □ 6</td> </tr> </tbody> </table> □ represents one line worth of spaces.	SPACE			Number of Lines and Space (□ represents space)	2	1	0	12	0	0	0	1 □ 10 □ 1	0	0	1	2 □ 8 □ 2	0	1	0	3 □ 6 □ 3	0	1	1	4 □ 4 □ 4	1	0	0	5 □ 2 □ 5	1	0	1	6 □ 6	1	1	0	6 □ □ 6	1	1	1	6 □ □ □ 6	Leave one line worth of space in the vertical direction. For example, 6 □ 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7. A lone is 18 X N horizontal scan lines. N is determined by the character size in the vertical direction as follows: x1 N = 1 x2 N = 2 x3 N = 3 x3 N = 3
		SPACE					Number of Lines and Space (□ represents space)																																								
2	1	0			12																																										
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C	SPACE1	⓪																																													
		1																																													
D	SPACE2	⓪																																													
		1																																													

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(4) Address 0123 H

DA	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	⓪	If VS is the horizontal display start location, $VS = H \times \left(\sum_{n=0}^9 2^n VP_n \right)$	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000000 ₂) setting is forbidden. Note 1: In case of B/F register is "0".
		1		
1	VP1	⓪	H: Cycle with the horizontal synchronizing pulse 1023 setting are possible.	
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5	⓪		
		1		
6	VP6	⓪		
		1		
7	VP7	⓪		
		1		
8	VP8	⓪		
		1		
9	VP9 (MSB)	⓪		
		1		
A	TEST0	⓪	Normally set to "0".	
		1	Test mode	
B	TEST1	⓪	Normally set to "0".	
		1	Test mode	
C	TEST2	⓪	Normally set to "0".	
		1	Test mode	
D	TEST3	⓪	Normally set to "0".	
		1	Test mode	

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(5) Address 0124 H

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 1.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
1	DSP1	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 2.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
2	DSP2	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 3.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
3	DSP3	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 4.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
4	DSP4	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 5.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
5	DSP5	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 6.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
6	DSP6	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 7.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
7	DSP7	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 8.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
8	DSP8	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 9.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
9	DSP9	⓪	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 10.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
A	DSP10	⓪	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 11.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
B	DSP11	⓪	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 12.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
C	TEST4	⓪	NOrmally set to "0".	
		1	Test mode	
D	TEST5	⓪	NOrmally set to "0".	
		1	Test mode	

Note 2 : Refer to DISPLAY FORM 1.

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(6) Address 0125 H

DA	Register	Contents		Remarks												
		Status	Function													
0	LIN2	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 2nd line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
1	LIN3	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 3rd line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
2	KIN4	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 4th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
3	LIN5	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 5th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
4	LIN6	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 6th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
5	LIN7	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 7th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
6	LIN8	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 8th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
7	LIN9	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 9th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
8	V1SZ0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 1st line. (display monitor 1 ~ 12 line)												
		1	<table border="1"> <thead> <tr> <th>V1SZ1</th> <th>V1SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		V1SZ1	V1SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
V1SZ1	V1SZ0	Vertical direction size														
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0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
9	V1SZ1	⓪														
		1														
A	VSZ1L0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 ~ LIN17.												
		1	<table border="1"> <thead> <tr> <th>VSZ1L1</th> <th>VSZ1L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ1L1	VSZ1L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ1L1	VSZ1L0	Vertical direction size														
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1	0	3H/dot														
1	1	4H/dot														
B	VSZ1L1	⓪														
		1														
C	VSZ1H0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 ~ LIN17.												
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VSZ1H1	VSZ1H0	Vertical direction size														
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0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
D	VSZ1H1	⓪														
		1														

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(7) Address 0126 H

DA	Register	Contents		Remarks												
		Status	Function													
0	LIN10	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 10th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
1	LIN11	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 11th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
2	KIN12	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 12th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
3	LIN13	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 13th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
4	LIN14	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 14th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
5	LIN15	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 15th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
6	LIN16	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 16th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
7	LIN17	⓪	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 17th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
8	V18SZ0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 18th line. (display monitor 1 ~ 12 line)												
		1	<table border="1"> <thead> <tr> <th>V18SZ1</th> <th>V18SZ0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		V18SZ1	V18SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
V18SZ1	V18SZ0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
9	V18SZ1	⓪														
		1														
A	VSZ2L0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 2 ~ 12 line) at "0" state in register LIN2 ~ LIN17.												
		1	<table border="1"> <thead> <tr> <th>VSZ2L1</th> <th>VSZ2L0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ2L1	VSZ2L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2L1	VSZ2L0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
B	VSZ2L1	⓪														
		1														
C	VSZ2H0	⓪	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 2 ~ 12 line) at "1" state in register LIN2 ~ LIN17.												
		1	<table border="1"> <thead> <tr> <th>VSZ2H1</th> <th>VSZ2H0</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1H/dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>2H/dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>3H/dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>4H/dot</td> </tr> </tbody> </table>		VSZ2H1	VSZ2H0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2H1	VSZ2H0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
D	VSZ2H1	⓪														
		1														

M52780-XXXSP

I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(8) Address 0127 H

DA	Register	Contents		Remarks																																				
		Status	Function																																					
0	RR	⓪	<table border="1"> <thead> <tr> <th>RB</th> <th>RG</th> <th>RR</th> <th>Color</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table>	RB	RG	RR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the color of all blanking.
		RB		RG	RR	Color																																		
0	0	0		Black																																				
0	0	1		Red																																				
0	1	0		Green																																				
0	1	1		Yellow																																				
1	0	0		Blue																																				
1	0	1		Magenta																																				
1	1	0		Cyan																																				
1	1	1		White																																				
1																																								
1	RG	⓪	<table border="1"> <thead> <tr> <th>BB</th> <th>BG</th> <th>BR</th> <th>Color</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table>	BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		BB		BG	BR	Color																																		
0	0	0		Black																																				
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2	RB	⓪	<table border="1"> <thead> <tr> <th>BSZ11</th> <th>BSZ10</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1H/dot</td></tr> <tr><td>0</td><td>1</td><td>2H/dot</td></tr> <tr><td>1</td><td>0</td><td>3H/dot</td></tr> <tr><td>1</td><td>1</td><td>4H/dot</td></tr> </tbody> </table>	BSZ11	BSZ10	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot																						
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3	FR	⓪		<table border="1"> <thead> <tr> <th>VSZ21</th> <th>VSZ20</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1H/dot</td></tr> <tr><td>0</td><td>1</td><td>2H/dot</td></tr> <tr><td>1</td><td>0</td><td>3H/dot</td></tr> <tr><td>1</td><td>1</td><td>4H/dot</td></tr> </tbody> </table>	VSZ21	VSZ20	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1		4H/dot																				
		VSZ21			VSZ20	Vertical direction size																																		
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1	0	3H/dot																																						
1	1	4H/dot																																						
1																																								
4	FG	⓪	Normally set to "0".																																					
		1																																						
5	FB	⓪				Normally set to "0".																																		
		1																																						
6	TEST6	⓪		Normally set to "0".																																				
		1																																						
7	TEST7	⓪							Normally set to "0".																															
		1																																						
8	TEST8	⓪									Normally set to "0".																													
		1																																						
9	BETA14	⓪	Matrix-outline display (12 x 18 dot)		Set this register to the character font set by display RAM BR, BG and BB.																																			
		1											Matrix-outline display (14 x 18 dot)																											
A	HSZ10	⓪			T: Display frequency cycle	Character size setting in the vertical direction for the first line.																																		
		1					<table border="1"> <thead> <tr> <th>HSZ11</th> <th>HSZ10</th> <th>Vertical direction size</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1H/dot</td></tr> <tr><td>0</td><td>1</td><td>2H/dot</td></tr> <tr><td>1</td><td>0</td><td>3H/dot</td></tr> <tr><td>1</td><td>1</td><td>4H/dot</td></tr> </tbody> </table>						HSZ11	HSZ10	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot													
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D	HSZ21	⓪		T: Display frequency cycle		Character size setting in the vertical direction for the 2nd line to 12th line.																																		
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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

(9) Address 0128 H

DA	Register	Contents		Remarks																		
		Status	Function																			
0	BCOL	①	Blanking of BLK0, BLK1	Sets all raster blanking																		
		1	All raster blanking																			
1	B/F	①	Synchronize with the leading edge of horizontal synchronization.	Synchronize with the front porch or back porch of the horizontal synchronazation signal.																		
		1	Synchronize with the trailing edge of horizontal synchronization.																			
2	VMASK	①	Do not mask by VERT input signal	This register has or do not have mask at phase comparison operating.																		
		1	Mask by VERT input signal																			
3	POLV	①	VERT pin polarity is negative electrode	Set VERT pin polarity																		
		1	VERT pin polarity is positive electrode																			
4	POLH	①	HOR pin polarity is negative electrode	Set HOR pin polarity																		
		1	HOR pin polarity is positive electrode																			
5	BLK0	①	<table border="1" style="display: inline-table; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="2">BLK</th> <th rowspan="2">Blanking mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>0</td> <td>Character size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Matrix-outline size</td> </tr> </tbody> </table>	BLK		Blanking mode	1	0	Matrix-outline size	0	0	Character size	0	1	Border size	1	0	Matrix-outline size	Set blanking mode. (Note 3) An example of blanking mode at BCOL = "0", DSPn = "0"(n = 0 ~ 11) shown left.			
BLK		Blanking mode																				
1	0		Matrix-outline size																			
0	0	Character size																				
0	1	Border size																				
1	0	Matrix-outline size																				
1																						
6	BLK1	①																				
7	SYAD	①	Border display of character	(Note 4)																		
		1	Shadow display of character																			
8	RAMERS	①	RAM not erased	There is no need to reset because there is no register for this bit.																		
		1	RAM erased																			
9	STOP	①	Oscillation of clock for display	R, G, B, and BLNK0 output can be altered.																		
		1	Stop the oscillation of clock for display																			
A	DSPON	①	Display OFF	Display can be altered.																		
		1	Display ON																			
B	BLINK0	①	<table border="1" style="display: inline-table; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="2">BLK</th> <th rowspan="2">Duty</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>Blinking OFF</td> </tr> <tr> <td>0</td> <td>0</td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </tbody> </table>	BLK		Duty	1	0	Blinking OFF	0	0		0	1	25%	1	0	50%	1	1	75%	Blinking duty ratio can be altered.
BLK		Duty																				
1	0		Blinking OFF																			
0	0																					
0	1	25%																				
1	0	50%																				
1	1	75%																				
1																						
C	BLINK1	①																				
D	BLINK2	①	Divided into 64 of vertical synchronous signal	Blinking frequency can be altered.																		
		1	Divided into 32 of vertical synchronous signal																			

Note 3: Refer to DISPLAY FORM 1
4: Refer to DISPLAY FORM 3

M52780-XXXSP

I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

DISPLAY FORM 1

Table 1 shows display form of blanking.

Table 1. Display mode

BCOL	Standard blanking		When the all of registers DSPn (Note 2) are set to "0"	When some of registers DSPi are set to "1"		BLNK0 output
	BLK1	BLK0		DSPn = 0	DSPn = 1	
0	0	0	Matrix-outline and border display. color set: FR,FG,FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR,FG,FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0"line DSPn = "0"line } Matrix-outline size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0"line → Border size DSPn = "0"line → Matrix-outline size
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	DSPn = "0"line → Matrix-outline size DSPn = "0"line → Character size
1 (Note 1)	0	0	Matrix-outline and border display. color set: FR,FG,FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR,FG,FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	All blanking size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	

Note 1: Color setting of raster area is set by register RR, RG, and RB.

2: DSPn (n = 0 - 11)

3: Set by BR, BG, and BB of display RAM.

4: Set border by register FR, FG, and FB. Set matrix-outline by BR, BG, and BB of display RAM.

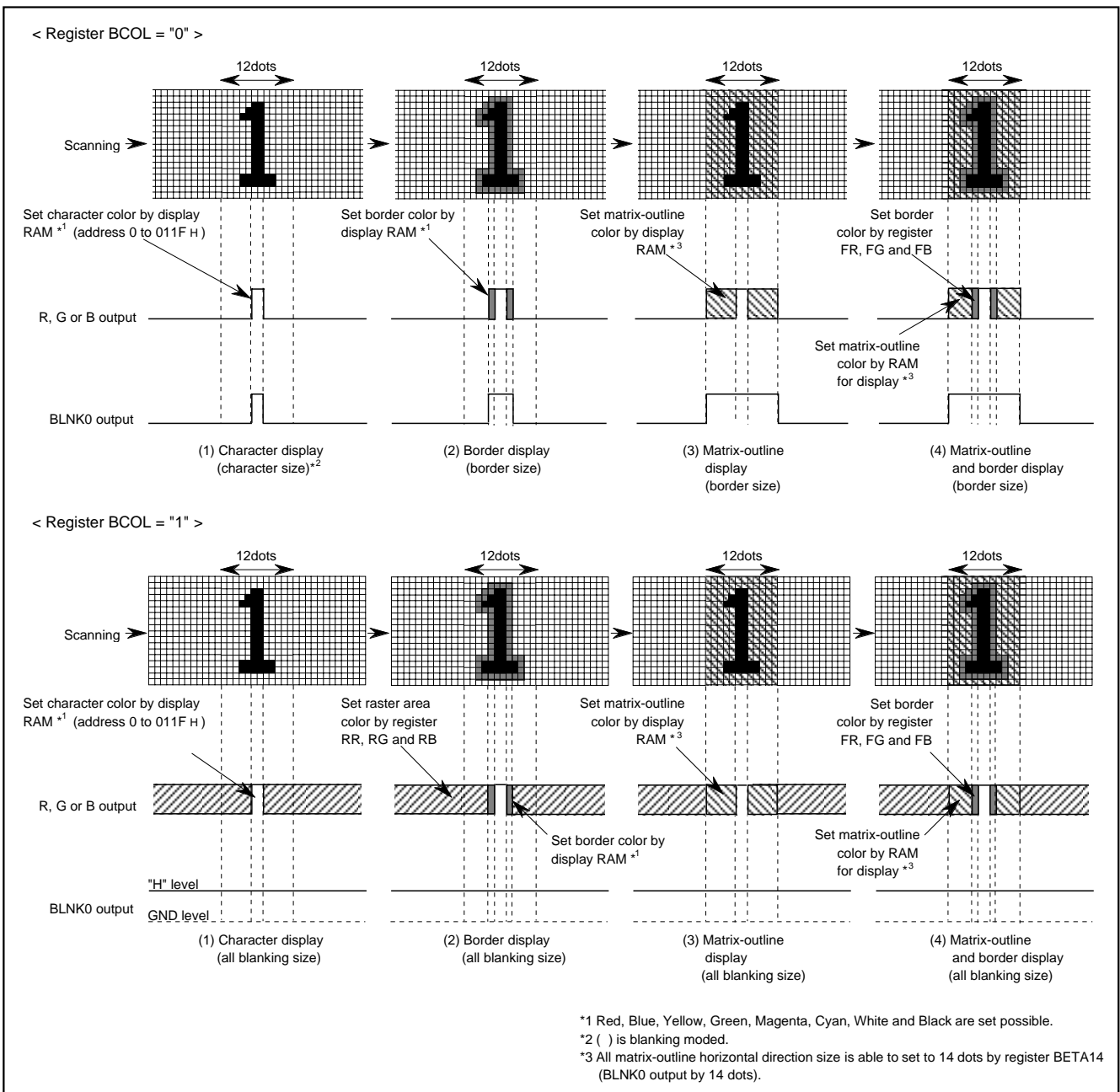
M52780-XXXSP

12C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

DISPLAY FORM 2

M52780SP has the following four display forms.

- (1) Character size
: Blanking same as the character size.
- (2) Border size
: Blanking the background as a size from character.
- (3) Matrix-outline size
: Blanking the background 12 x 18 dot.
When set register BETA14 to "1", setting of blanking the background 14 x 18 dot is possible.
- (4) All blanking size
: When set register BCOL to "1", all raster area is blanking.

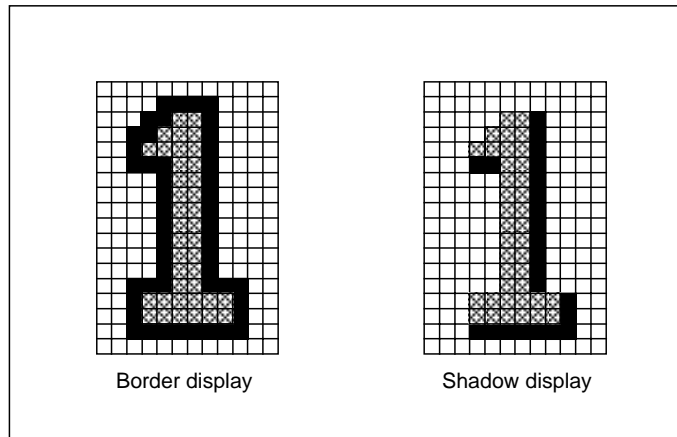


Display form

DISPLAY FORM 3

When border display mode, if set SYAD = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.



Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

M52780-XXXSP

I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the I2C input function. Example of data setting is shown in Figure 5.

Example of data setting by the serial input function (M52780SP)

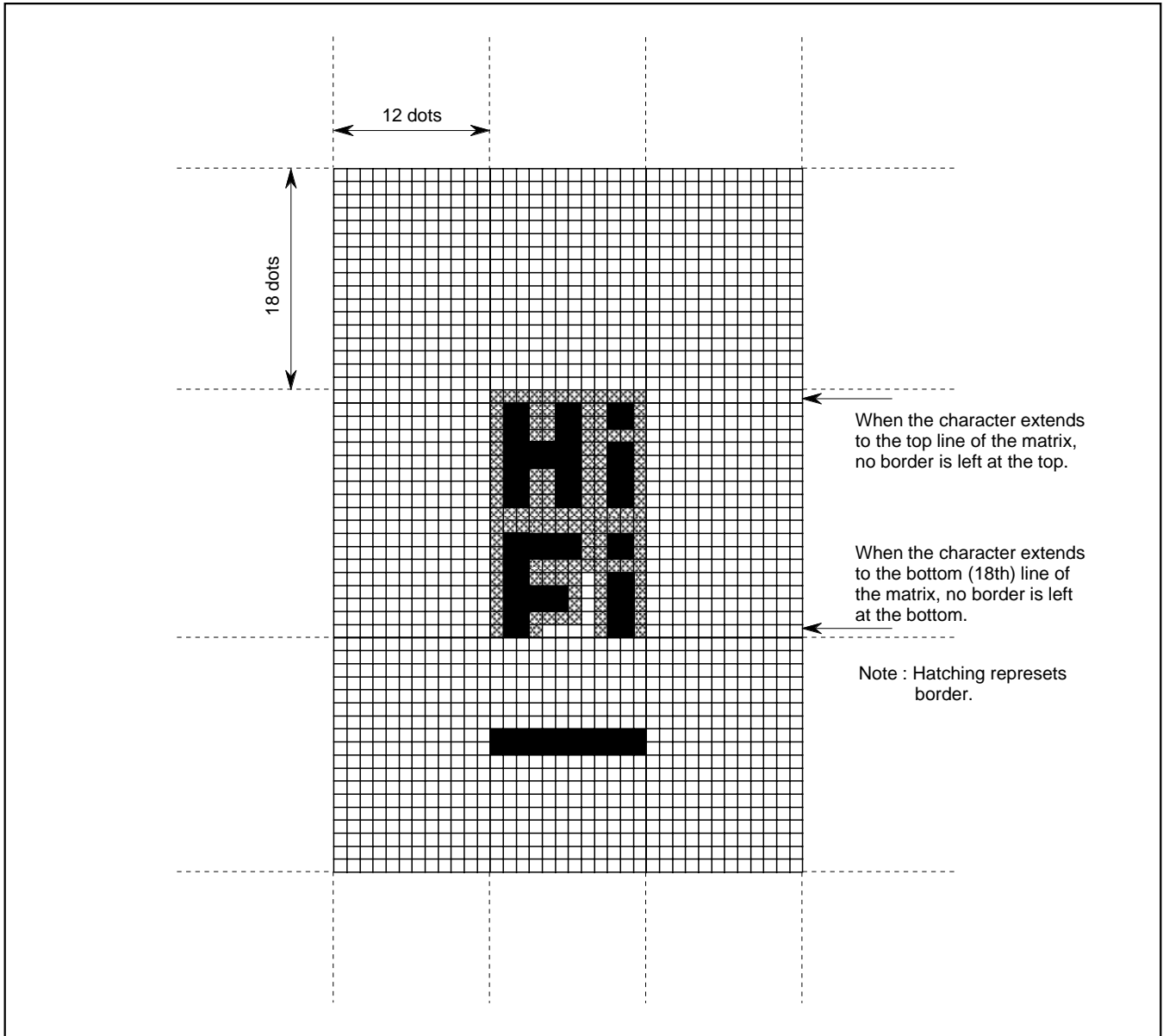
		Upper 8 bits (ADDRESS2 or DATA n2)								Lower 8 bits (ADDRESS1 or DATA n1)								
		DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Addition
		200 msec hold																System set-up
1	address 0120H	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address set
2	deta 0120H	0	0	0	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Setting frequency dividing value (Note 1)
3	deta 0121H	0	0	0	0	1	0	1	0	1	1	1	0	1	0	1	1	Output setting
4	deta 0122H	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting
5	deta 0123H	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting
6	deta 0124H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting
7	deta 0125H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
8	deta 0126H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting
9	deta 0127H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting
10	deta 0128H	0	0	0	0	0	0	0	1	0	1	1	POLH	POLV	0	0	0	Display OFF, display form (Note 2)
		20 msec hold																
11	deta 0000H	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	Character setting
12	⋮	⋮	Character background color			⋮	Character color			Character code								
297	⋮	⋮				⋮												
298	deta 011FH	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0	
299	address 0128H	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	Address setting
300	deta 0128H	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON, display form (Note 2)

Note 1: Input horizontal synchronous signal to HOR pin.
 Note 2: Matrix-outline display in this data.

Example of data setting by the I2C input function

CHARACTER FONT

Images are composed on a 12 X 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.



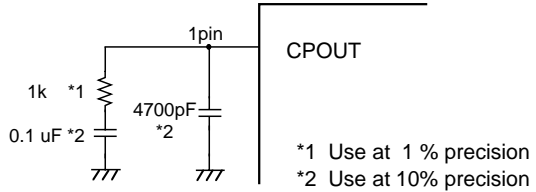
Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction

Character code FFH is fixed as a blank without background.
Therefore, you cannot register a character font in this code.

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/Output	Function
9	CPOUT	Phase difference	Output	<p>Connect loop filter to this pin.</p>  <p>*1 Use at 1 % precision *2 Use at 10% precision</p>
12	VIN	Vertical synchronization signal input	Input	This pin inputs the vertical synchronizatin signal. Hysteresis input.
13	HIN	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronizatin signal. Hysteresis input.
17	$\overline{\text{AC}}$	Auto-clear input	Input	When "L", this pin resets the internal IC circuit.Hysteresis input. Includes built-in pull-up resistor.

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I2C BUS CONTROLLED 3CH VIDEO PRE-AMP WITH OSD CONTROLLER FOR HIGH RESOLUTION COLOR DISPLAY MONITOR

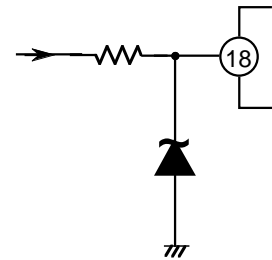
Application Method

CLAMP PULSE INPUT

Clamp pulse width is recommended

above 15 KHz, 1.0 μ secabove 30 KHz, 0.5 μ secabove 64 KHz, 0.3 μ sec .

The clamp pulse circuit in ordinary set is a long round about way, and beside high voltage, sometimes connected to external terminal, it is very easy affected by large surge. Therefore, the Fig. shown right is recommended.



Notice of application

- Make the nearest distance between output pin and pull down resistor.
- Recommended pedestal voltage of IC output signal is 2V.

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APPLICATION EXAMPLE

